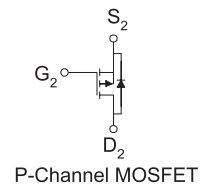
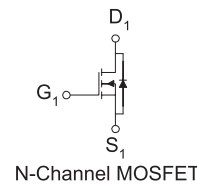
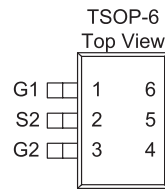


N & P-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.047 @ $V_{GS} = 4.5V$	4.1
	0.055 @ $V_{GS} = 2.5V$	3.8
-20	0.079 @ $V_{GS} = -4.5V$	-3.2
	0.110 @ $V_{GS} = -2.5V$	-2.7



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V _{DS}	20	-20	V
Gate-Source Voltage		V _{GS}	±8	±8	
Continuous Drain Current ^a	T _A =25°C	I _D	4.1	-3.2	A
	T _A =70°C		3.3	-2.6	
Pulsed Drain Current ^b		I _{DM}	8	-8	
Continuous Source Current (Diode Conduction) ^a		I _S	1.05	-1.05	A
Power Dissipation ^a	T _A =25°C	P _D	1.15		W
	T _A =70°C		0.7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ	Max	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	93	110	93	110	$^\circ\text{C/W}$
	Steady State	130	150	130	150	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

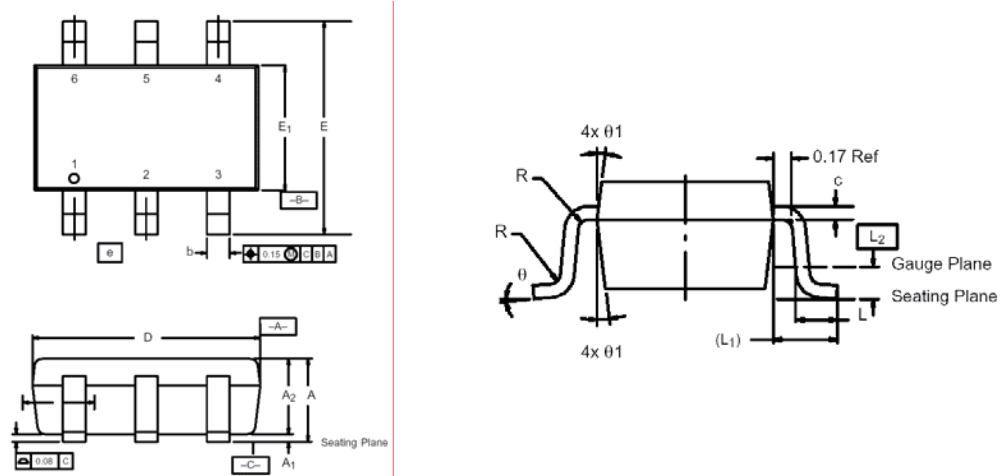
SPECIFICATIONS (T _A = 25° C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	0.4			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-0.4			
Gate-Body Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 8 V	N			100	uA
		V _{DS} = 0 V, V _{GS} = -8 V	P			-100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N			1	uA
		V _{DS} = -16 V, V _{GS} = 0 V	P			-1	
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C	N			10	uA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C	P			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N	5			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P	-5			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.1 A	N			0.047	Ω
		V _{GS} = -4.5 V, I _D = -3.2 A	P			0.079	
		V _{GS} = 2.5 V, I _D = 3.8 A	N			0.055	
		V _{GS} = -2.5 V, I _D = -2.7 A	P			0.110	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 5 V, I _D = 4.1 A	N		10		S
		V _{DS} = -5 V, I _D = -3.2 A	P		5		
Diode Forward Voltage ^A	V _{SD}	I _S = 1.05 A, V _{GS} = 0 V	N		0.80		S
		I _S = -1.05 A, V _{GS} = 0 V	P		-0.83		
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =4.1A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3.2A	N		7.5		nC
			P		3.8		
Gate-Source Charge	Q _{gs}		N		0.6		
			P		0.6		
Gate-Drain Charge	Q _{gd}		N		1.0		
			P		1.5		
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =4.5V, I _D =1A , R _{GEN} =15Ω, P-Channel V _{DD} =-15V, V _{GS} =-4.5V, I _D =-1A R _{GEN} =15Ω	N		5		nS
Rise Time	t _r		P		5		
			N		12		
			P		15		
Turn-Off Delay Time	t _{d(off)}		N		13		
			P		20		
Fall-Time	t _f		N		7		
			P		20		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Package Information

TSOP-6: 6LEAD



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	—	1.10	0.036	—	0.043
A ₁	0.01	—	0.10	0.0004	—	0.004
A ₂	0.84	—	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
L	0.35	—	0.50	0.014	—	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		