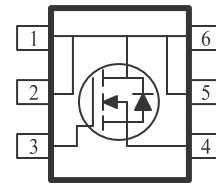
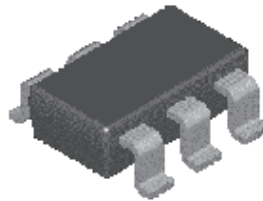


N-Channel 60V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Low Gate Charge
- Fast Switch
- Miniature TSOP-6 Surface Mount Package Saves Board Space

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.092 @ $V_{GS} = 10\text{ V}$	3.4
	0.107 @ $V_{GS} = 4.5\text{ V}$	3.1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	3.4	A
	$T_A = 70^\circ\text{C}$		2.7	
Pulsed Drain Current ^b		I_{DM}	± 15	
Continuous Source Current (Diode Conduction) ^a		I_S	1.7	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.0	W
	$T_A = 70^\circ\text{C}$		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5\text{ sec}$	R_{THJA}	62.5	$^\circ\text{C/W}$
	Steady-State		110	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48 V, V _{GS} = 0 V			1	uA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 55°C			50	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	10			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.4 A			92	mΩ
		V _{GS} = 4.5 V, I _D = 3.1 A			107	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 4.5 V, I _D = 3.4 A		8		S
Diode Forward Voltage	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		1.10		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 5 V, I _D = 3.4 A		3.6		nC
Gate-Source Charge	Q _{gs}			1.8		
Gate-Drain Charge	Q _{gd}			1.3		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω, I _D = 1 A, V _{GEN} = 10 V		10		ns
Rise Time	t _r			10		
Turn-Off Delay Time	t _{d(off)}			20		
Fall-Time	t _f			10		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.