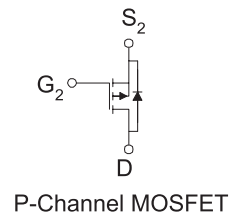
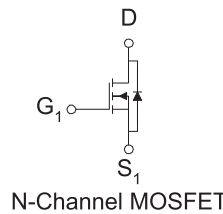
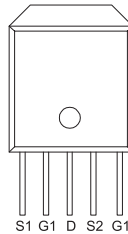


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	95 @ $V_{GS} = 2.5V$	20
	59 @ $V_{GS} = 4.5V$	24
-26.5	178 @ $V_{GS} = -2.5V$	-14
	118 @ $V_{GS} = -4.5V$	-17

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-26.5	V
Gate-Source Voltage		V_{GS}	± 12	± 12	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	24	-17	A
Pulsed Drain Current ^b		I_{DM}	40	-40	
Continuous Source Current (Diode Conduction) ^a		I_S	30	-30	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	0.6			V
		V _{GS} = V _{DS} , I _D = -250 uA	P	-0.6			
Gate-Body Leakage	I _{GSS}	V _{GS} = -12 V, V _{DS} = 0 V	P			±100	nA
		V _{GS} = 12 V, V _{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA
		V _{DS} = 24 V, V _{GS} = 0 V	N			1	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N	20			A
		V _{DS} = -5 V, V _{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5.0 A	N			59	mΩ
		V _{GS} = 2.5 V, I _D = 4.2 A				95	
		V _{GS} = -4.5 V, I _D = -3.6 A	P			112	
		V _{GS} = -2.5 V, I _D = -2.9 A				172	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 5.0 A	N		25		S
		V _{DS} = -15 V, I _D = -3.6 A	P		10		
Dynamic							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =5.0A	N		6.3		nC
Gate-Source Charge	Q _{gs}		P		10		
		Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3.6A	N		
P					2.2		
			N		1.9		
			P		1.7		
Switching							
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =4.5V, I _D =1A , R _{GEN} =6Ω,	N		7.4		nS
Rise Time	t _r		P		7.6		
		Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} =-15V, V _{GS} =-4.5V, I _D =-1A R _{GEN} =6Ω	N		
P					6.8		
Fall-Time	t _f	N		22.2			
		P		33.6			
		N		3.6			
		P		23.2			

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

