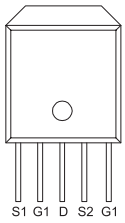
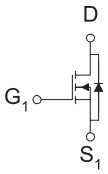
P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

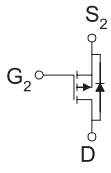
- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature DPAK Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	20 @ V_{GS} = 4.5V	51
	16 @ V_{GS} = 10V	41
-30	33 @ V_{GS} = -4.5V	-41
	23 @ V_{GS} = -10V	-31





N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	20	-20	
Continuous Drain Current[a]	T_A=25°C	I_D	51	-41.0	A
Pulsed Drain Current[b]		I_{DM}	±40	±40	
Continuous Source Current (Diode Conduction)[a]		I_S	30	-30	A
Power Dissipation[a]	T_A=25°C	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

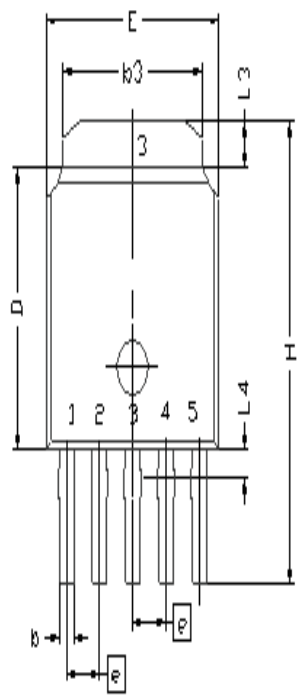
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	1			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-1			
Gate-Body Leakage	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	P			±100	nA
		V_{GS} = 20 V, V_{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V	P			-1	uA
		V_{DS} = 24 V, V_{GS} = 0 V	N			1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -10 V	P	-50			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	N			16	mΩ
		V_{GS} = 4.5 V, I_D = 8.4 A				20	
		V_{GS} = -10 V, I_D = -8.5 A	P			23	
		V_{GS} = -4.5 V, I_D = -6.8 A				33	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	N		40		S
		V_{DS} = -15 V, I_D = -9.5 A	P		31		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=10A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-10A	N		12		nC
			P		13		
Gate-Source Charge	Q_{gs}		N		3.3		
			P		5.8		
Gate-Drain Charge	Q_{gd}		N		4.5		
			P		12		
Switching							
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=10V, I_D=1A , R_{GEN}=25Ω, P-Channel V_{DD}=-15V, V_{GS}=-10V, I_D=-1A R_{GEN}=15Ω	N		20		nS
			P		15		
Rise Time	t_r		N		9		
			P		16		
Turn-Off Delay Time	$t_{d(off)}$		N		70		
			P		62		
Fall-Time	t_f		N		20		
			P		46		

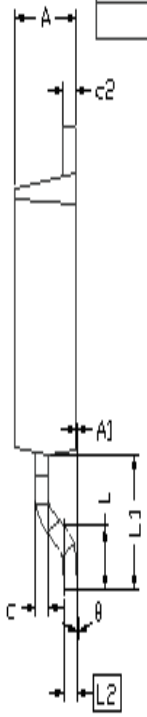
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

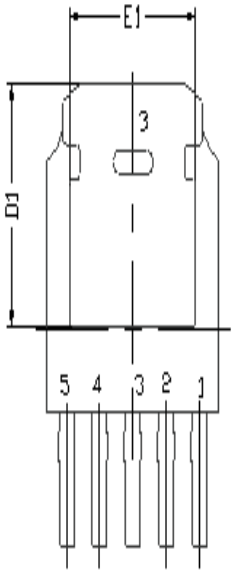
b. Guaranteed by design, not subject to production testing.

ECN #	REV.	DATE	DESCRIPTION	DRG.	APPR.
G-12057	A	01/17/05	NEW ISSUE		





SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.38	0.50	0.62
b3	5.21	5.34	5.46
e	1.300BSC		
A	2.20	2.30	2.38
A1	--	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.20	--	--
E1	4.40	--	--
θ	0°	--	10°



GEM Electronics (Shanghai)

DRAWN BY: X.G.ZENG	TITLE: D-PAK 5L CASE OUTLINE
DATE: 2005.01.17	
APPROVED:	
SCALE: NTS	DRAWING NUMBER: A010-402-00 REV: A