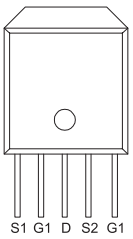
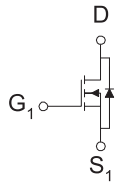
P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

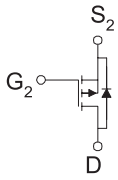
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	45 @ V_{GS} = 2.5V	29
	35 @ V_{GS} = 4.5V	36
-26.5	70 @ V_{GS} = -2.5V	-20
	52 @ V_{GS} = -4.5V	-26

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology





N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-26.5	V
Gate-Source Voltage		V_{GS}	±12	±12	
Continuous Drain Current[a]	T_A=25°C	I_D	36	-26	A
	T_A=70°C		30	-21	
Pulsed Drain Current[b]		I_{DM}	40	-40	
Continuous Source Current (Diode Conduction)[a]		I_S	30	-30	A
Power Dissipation[a]	T_A=25°C	P_D	50	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

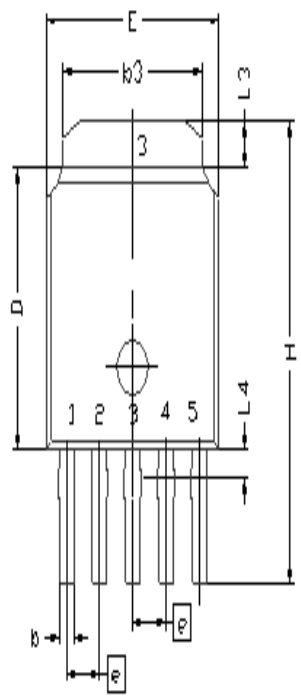
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	0.6			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-0.6			
Gate-Body Leakage	I_{GSS}	V_{GS} = -12 V, V_{DS} = 0 V	P			±100	nA
		V_{GS} = 12 V, V_{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V	P			-1	uA
		V_{DS} = 24 V, V_{GS} = 0 V	N			1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 4.5 V, I_D = 6.9 A	N			35	mΩ
		VGS = 2.5 V, I_D = 6 A				45	
		VGS = -4.5 V, I_D = -5.2 A	P			52	
		VGS = -2.5 V, I_D = -4.2 A				70	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 6.9 A	N		25		S
		V_{DS} = -15 V, I_D = -5.2 A	P		10		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=6.9A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-5.2A	N		6.0		nC
			P		25		
Gate-Source Charge	Q_{gs}		N		1.0		
			P		2.4		
Gate-Drain Charge	Q_{gd}		N		1.5		
			P		3.9		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=4.5V, I_D=1A , R_{GEN}=6Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=6Ω	N		7.4		nS
			P		7.6		
Rise Time	t_r		N		4		
			P		6.8		
Turn-Off Delay Time	$t_{d(off)}$		N		22.2		
			P		33.6		
Fall-Time	t_f		N		3.6		
			P		23.2		

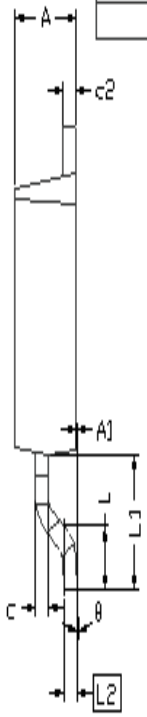
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

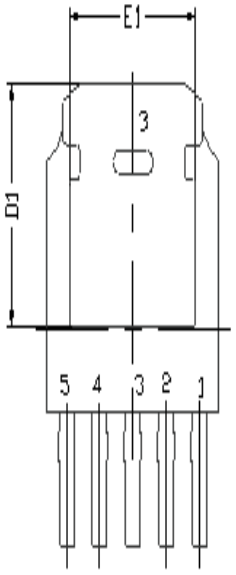
b. Guaranteed by design, not subject to production testing.

ECN #	REV.	DATE	DESCRIPTION	DRG.	APPR.
G-12057	A	01/17/05	NEW ISSUE		





SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.38	0.50	0.62
b3	5.21	5.34	5.46
e	1.300BSC		
A	2.20	2.30	2.38
A1	--	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.20	--	--
E1	4.40	--	--
θ	0°	--	10°



GEM Electronics (Shanghai)

DRAWN BY: X.G.ZENG	TITLE: D-PAK 5L CASE OUTLINE
DATE: 2005.01.17	
APPROVED:	
SCALE: NTS	DRAWING NUMBER: A010-402-00 REV: A