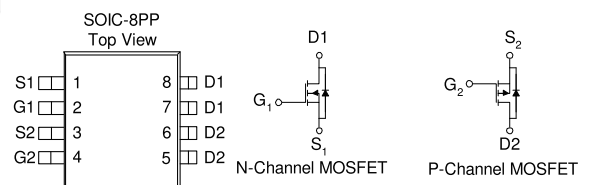


P & N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	58 @ $V_{GS} = 4.5V$	6.4
	82 @ $V_{GS} = 2.5V$	5.4
-30	112 @ $V_{GS} = -4.5V$	-4.6
	172 @ $V_{GS} = -2.5V$	-3.7

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	8	-8	
Continuous Drain Current ^a	I_D	6.4	-4.6	A
		5.2	-3.8	
Pulsed Drain Current ^b	I_{DM}	± 20	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	2.9	-2.9	A
Power Dissipation ^a	P_D	3.5	3.5	W
		2.2	2.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	35	$^\circ C/W$
		85	$^\circ C/W$

Notes

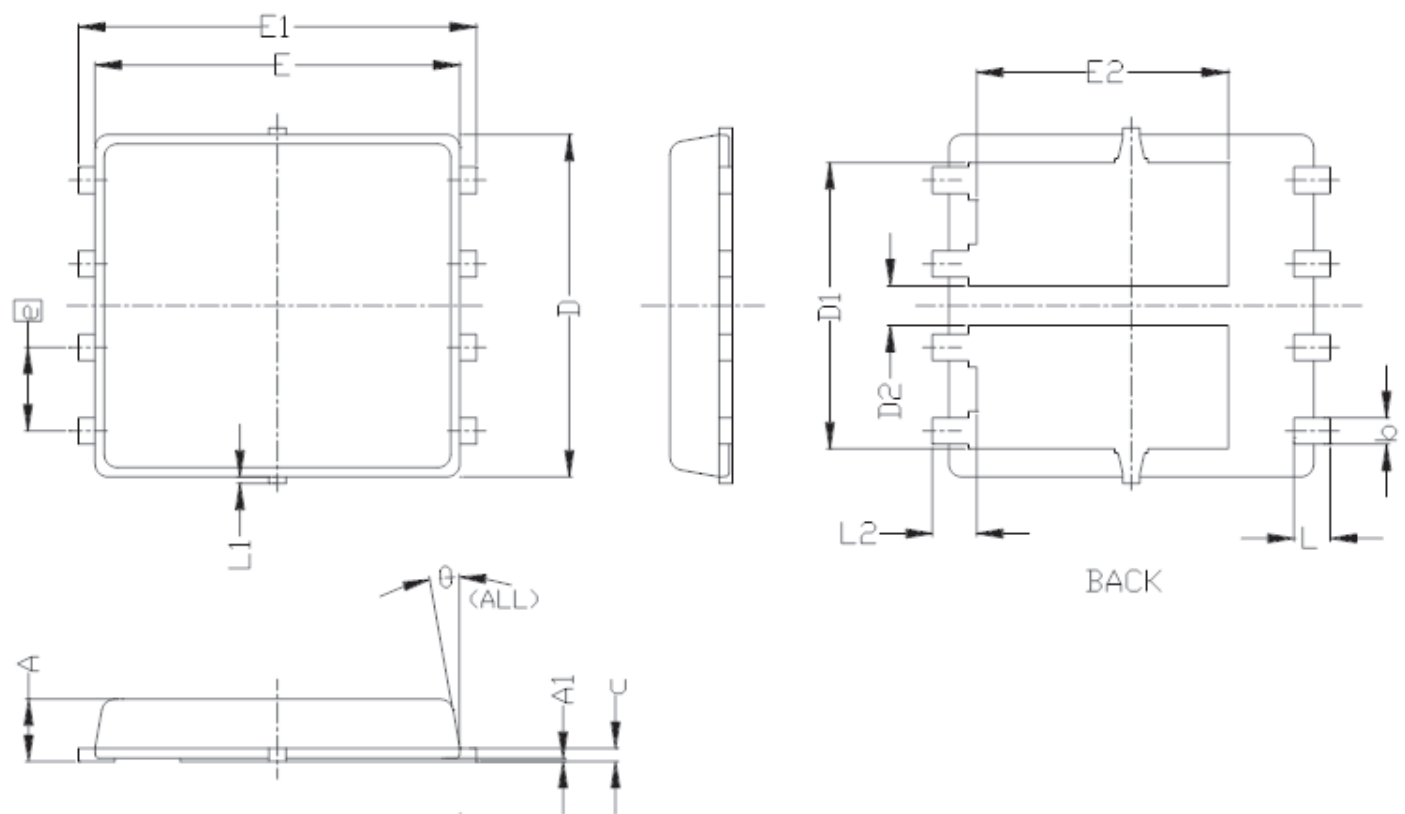
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits				Unit	
			Ch	Min	Typ	Max		
Static								
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 uA	N	0.3			V	
		V _{GS} = V _{DS} , I _D = -250 uA	P	-0.3				
Gate-Body Leakage	I _{GSS}	V _{GS} = 8 V, V _{DS} = 0 V	N			±100	nA	
		V _{GS} = -8 V, V _{DS} = 0 V	P			±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V	P			-1	uA	
		V _{DS} = 24 V, V _{GS} = 0 V	N			1		
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N	20			A	
		V _{DS} = -5 V, V _{GS} = -10 V	P	-20				
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A	N			58	mΩ	
		V _{GS} = 2.5 V, I _D = 1 A				82		
		V _{GS} = -4.5 V, I _D = -1 A	P			112		
		V _{GS} = -2.5 V, I _D = -1 A				172		
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 1 A	N		40		S	
		V _{DS} = -15 V, I _D = -1 A	P		31			
Dynamic								
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, V _{GS} =4.5V, I _D =1A P-Channel V _{DS} =-15V, V _{GS} =-4.5V, I _D =-1A	N		6		nC	
Gate-Source Charge	Q _{gs}		P		7			
Gate-Drain Charge	Q _{gd}		N		1			
			P		1			
Turn-On Delay Time	t _{d(on)}	N-Chaneel V _{DD} =15V, V _{GS} =5V, I _D =1A , R _{GEN} =25Ω, P-Channel V _{DD} =-15V, V _{GS} =-5V, I _D =-1A R _{GEN} =15Ω	N		9		nS	
Rise Time	t _r		P		6			
			N		15			
			P		13			
Turn-Off Delay Time	t _{d(off)}		N		40			
			P		20			
Fall-Time	t _f		N		10			
			P		10			

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	—	0.05	0.000	—	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D1	4.35 BSC			0.171 BSC		
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	3.625 BSC			0.143 BSC		
E3	1.275 BSC			0.050 BSC		
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	—	0.15	0	—	0.006
L2	0.68 REF			0.027 REF		
θ	0°	—	10°	0°	—	10°