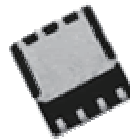


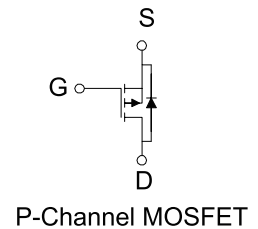
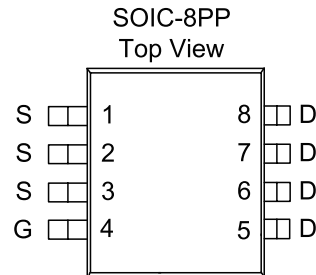
P-Channel 80-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8PP saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-80	75 @ $V_{GS} = -10V$	-6.7
	90 @ $V_{GS} = -4.5V$	-6.1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-80	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-6.7	A
	$T_A = 70^\circ\text{C}$		-5.0	
Pulsed Drain Current ^b		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	-2.1	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5.0	W
	$T_A = 70^\circ\text{C}$		3.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	$R_{\theta JA}$	25	$^\circ\text{C/W}$
	Steady State		65	$^\circ\text{C/W}$

Notes

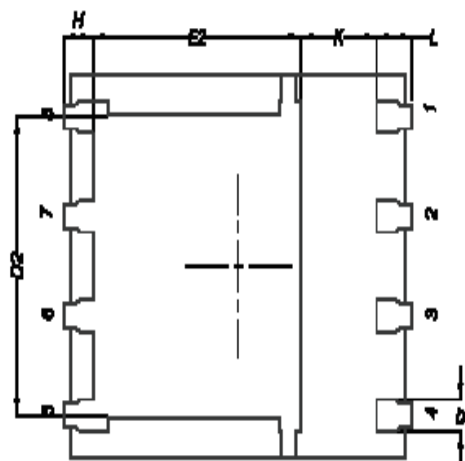
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 uA	-30			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-1			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -64 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -64 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-50			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -10 V, I _D = -6.7 A			75	mΩ
		V _{GS} = -4.5 V, I _D = -6.1 A			90	
Forward Tranconductance ^A	g _{fs}	V _{DS} = -15 V, I _D = -6.7 A		29		S
Diode Forward Voltage	V _{SD}	I _S = 2.5 A, V _{GS} = 0 V		-0.8		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -5 V, I _D = -6.7 A		25		nC
Gate-Source Charge	Q _{gs}			11		
Gate-Drain Charge	Q _{gd}			17		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 6 Ω , I _D = -1 A, V _{GEN} = -10 V		15		nS
Rise Time	t _r			13		
Turn-Off Delay Time	t _{d(off)}			100		
Fall-Time	t _f			54		

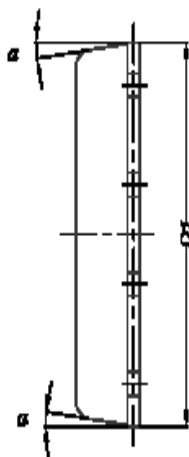
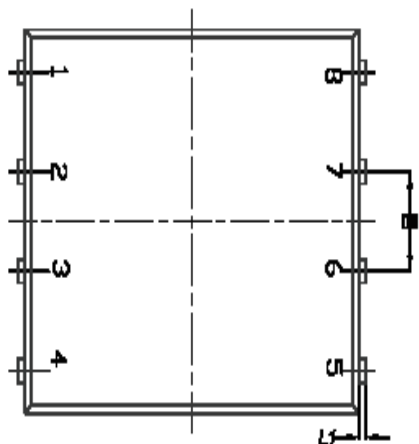
Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Package Information



BACKSIDE VIEW



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.90	4.90	5.00
D2	3.81	3.81	3.98
E	5.00	6.00	8.10
E1	5.70	6.75	5.00
E2	3.98	3.98	3.78
Ø	1.27 BSC		
H	0.41	0.51	0.81
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.08	0.13	0.20
α	0°	-	12°