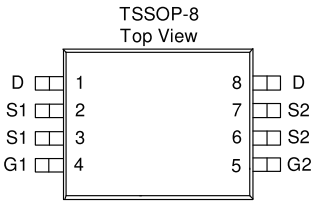
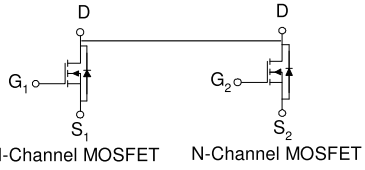
Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
20	0.028 @ V_{GS} = 4.5 V	6.8
	0.040 @ V_{GS} = 2.5V	5.8

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSSOP-8 saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	6.8	A
	T_A=70°C		5.4	
Pulsed Drain Current[b]		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	1.5	A
Power Dissipation[a]	T_A=25°C	P_D	1.2	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typ**	**Max**	
Maximum Junction-to-Ambient[a]	t <= 10 sec	R_{thJA}	72	83	°C/W
	Steady State		100	120	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	0.3			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	uA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			10	uA
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	30			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1 A			0.028	Ω
		V_{GS} = 2.5 V, I_D = 1 A			0.040	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 10 V, I_D = 1 A		25		S
Diode Forward Voltage[A]	V_{SD}	I_S = 1 A, V_{GS} = 0 V		0.89		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS}=10V, V_{GS}=4.5V, I_D=1A		6		nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=10V, V_{GS}=4.5V, I_D=1A , R_{GEN}=10Ω		8		nS
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			30		
Fall-Time	t_f			10		

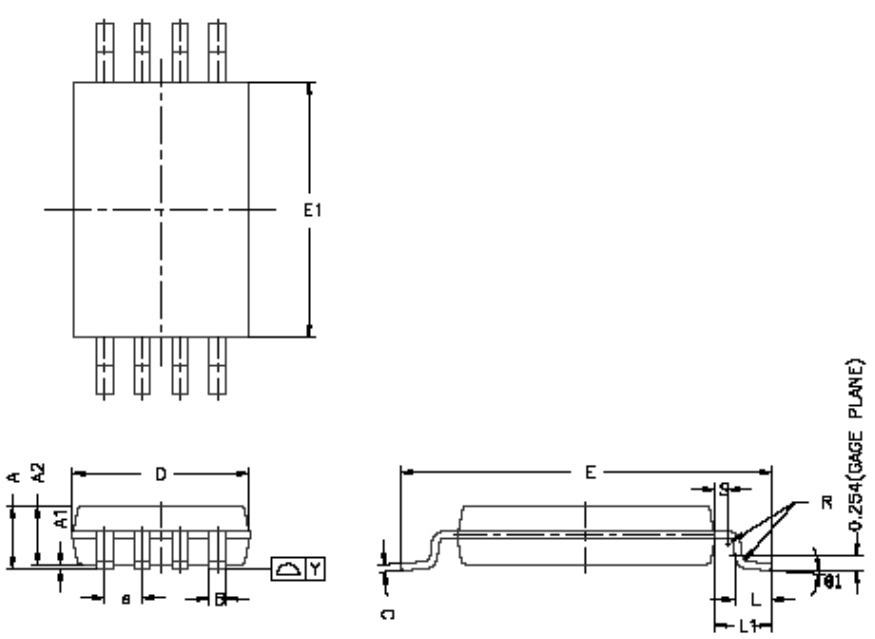
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	--	0.127	--
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	--	--	0.10
θ1	0°	4°	8°
R	0.09	--	--
S	0.20	--	--