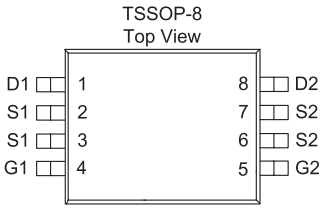
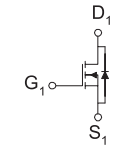
P & N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

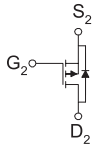
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	32 @ V_{GS} = 10V	4.3
	46 @ V_{GS} = 4.5V	3.7
-30	52 @ V_{GS} = -10V	-3.8
	80 @ V_{GS} = -4.5V	-2.8

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSSOP-8 saves board space
- Fast switching speed
- High performance trench technology





N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	4.3	-3.8	A
	T_A=70°C		3.5	-3.0	
Pulsed Drain Current[b]		I_{DM}	20	-20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.0	-1.0	A
Power Dissipation[a]	T_A=25°C	P_D	1.14	1.14	W
	T_A=70°C		0.73	0.73	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient[a]	t <= 10 sec	R_{thJA}	88	110	°C/W
	Steady State		120	150	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)							
Parameter	**Symbol**	**Test Conditions**	**Limits**				**Unit**
			Ch	**Min**	**Typ**	**Max**	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	1.0			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-1.0			
Gate-Body Leakage	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	N			±100	nA
		V_{GS} = -20 V, V_{DS} = 0 V	P			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N			1	uA
		V_{DS} = -16 V, V_{GS} = 0 V	P			-1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -10 V	P	-20			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 10 V, I_D = 4.3 A	N			32	mΩ
		VGS = 4.5 V, I_D = 3.7 A				46	
		VGS = -10 V, I_D = -3.8 A	P			52	
		VGS = -4.5 V, I_D = -2.8 A				80	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 4.3 A	N		11		S
		V_{DS} = -15 V, I_D = -3.8 A	P		11		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=4.3A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-3.8A	N		4.7		nC
			P		8.0		
Gate-Source Charge	Q_{gs}		N		1.8		
			P		2.3		
Gate-Drain Charge	Q_{gd}		N		1.5		
			P		4.5		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=4.5V, I_D=1A , R_{GEN}=6Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=6Ω	N		13		nS
			P		14		
Rise Time	t_r		N		14		
			P		14		
Turn-Off Delay Time	$t_{d(off)}$		N		30		
			P		40		
Fall-Time	t_f		N		30		
			P		30		

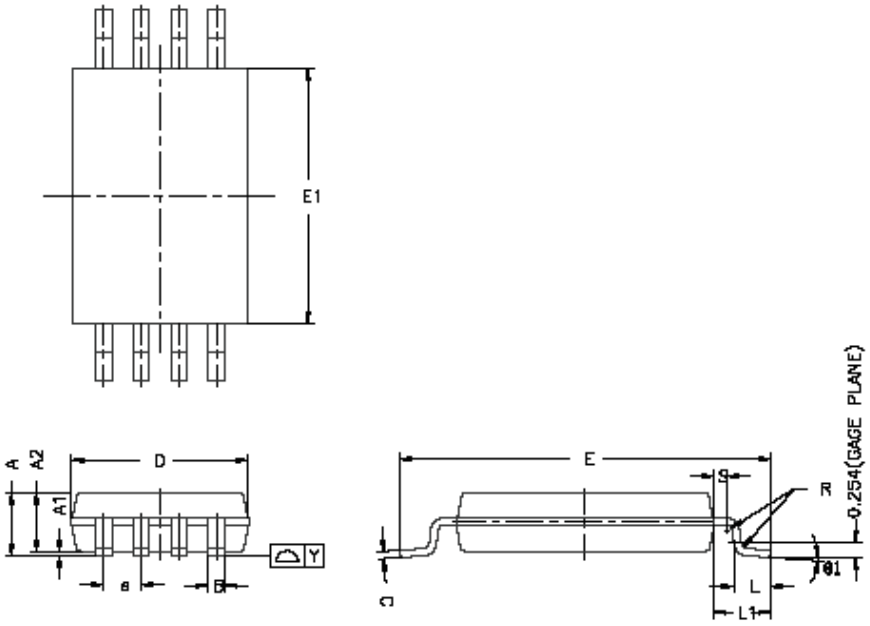
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NDM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	--	0.127	--
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	--	--	0.10
θ1	0°	4°	8°
R	0.09	--	--
S	0.20	--	--