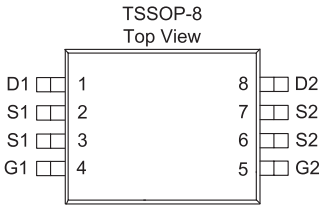
P & N-Channel 20-V (D-S) MOSFET

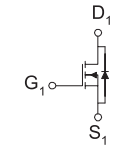
These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TSSOP-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

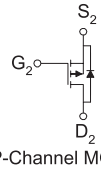
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	47 @ V_{GS} = 4.5V	4.7
	66 @ V_{GS} = 2.5V	3.9
	95 @ V_{GS} = 1.8V	3.3
-20	47 @ V_{GS} = -4.5V	-4.7
	72 @ V_{GS} = -2.5V	-3.8
	95 @ V_{GS} = -1.8V	-3.3





N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)

Parameter		Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	8	-8	
Continuous Drain Current[a]	T_A=25°C	I_D	4.7	-4.7	A
	T_A=70°C		3.8	-3.8	
Pulsed Drain Current[b]		I_{DM}	±50	±50	
Continuous Source Current (Diode Conduction)[a]		I_S	2.3	-2.3	A
Power Dissipation[a]	T_A=25°C	P_D	2.1	2.1	W
	T_A=70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	-55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient[a]	t <= 10 sec	R_{thJA}	72	83	°C/W
	Steady State		100	120	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	0.4			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-0.4			
Gate-Body Leakage	I_{GSS}	V_{GS} = -8 V, V_{DS} = 0 V	P			±100	nA
		V_{GS} = 8 V, V_{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V	P			-1	uA
		V_{DS} = 16 V, V_{GS} = 0 V	N			1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 4.5 V, I_D = 4.7 A	N			47	mΩ
		VGS = 2.5 V, I_D = 3.9 A				66	
		VGS = 1.8 V, I_D = 3.3 A				95	
		VGS = -4.5 V, I_D = -4.7 A	P			47	
		VGS = -2.5 V, I_D = -3.8 A				72	
		VGS = -1.8 V, I_D = -3.3 A				95	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	N		40		S
		V_{DS} = -15 V, I_D = -9.5 A	P		31		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=4.7A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4.7A	N		7.0		nC
			P		12.0		
Gate-Source Charge	Q_{gs}		N		1.1		
			P		2.0		
Gate-Drain Charge	Q_{gd}		N		2.0		
			P		2.0		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=4.5V, I_D=1A , R_{GEN}=25Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=15Ω	N		8		nS
			P		10		
Rise Time	t_r		N		24		
			P		20		
Turn-Off Delay Time	$t_{d(off)}$		N		35		
			P		31		
Fall-Time	t_f		N		10		
			P		21		

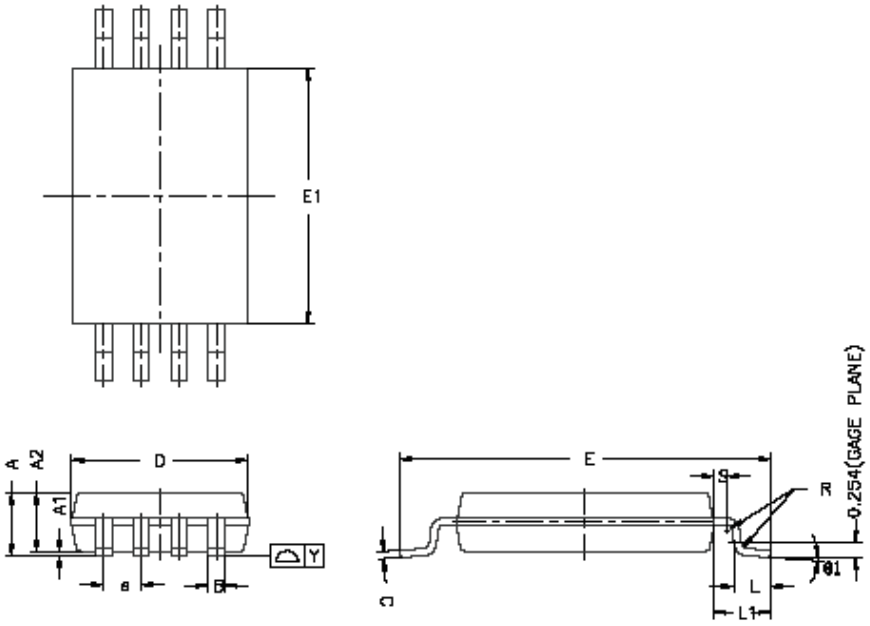
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NDM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	--	0.127	--
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	--	--	0.10
θ1	0°	4°	8°
R	0.09	--	--
S	0.20	--	--