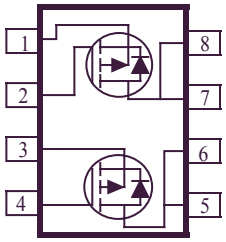
Dual P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (±25) for battery pack applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.021 @ V_{GS} = -10V	-7.8
	0.035 @ V_{GS} = -4.5V	-6.0



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current[a]	T_A=25°C	I_D	-7.8	A
	T_A=70°C		-6.2	
Pulsed Drain Current[b]		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[a]		I_S	-1.7	A
Power Dissipation[a]	T_A=25°C	P_D	2.0	W
	T_A=70°C		1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W
	Steady-State		110	°C/W

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-1		-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	uA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 55°C			-5	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-40			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -7.8 A		19	21	mΩ
		V_{GS} = -4.5 V, I_D = -6.0 A		28	35	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -10 V, I_D = -7.8 A		22		S
Diode Forward Voltage	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		-0.7	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -15 V, V_{GS} = -5 V, I_D = -7.8 A		15		nC
Gate-Source Charge	Q_{gs}			5.2		
Gate-Drain Charge	Q_{gd}			5.8		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 6 Ω , ID = -1 A, VGEN = -10 V		15		nS
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			62		
Fall-Time	t_f			46		

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics (P-Channel)

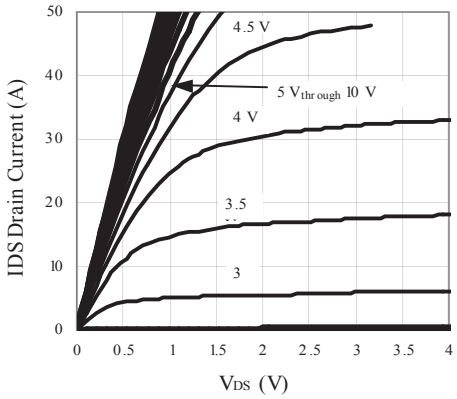


Figure 1. Output Characteristics

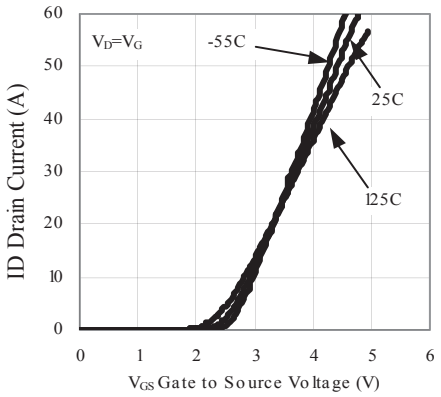


Figure 2. Transfer Characteristics

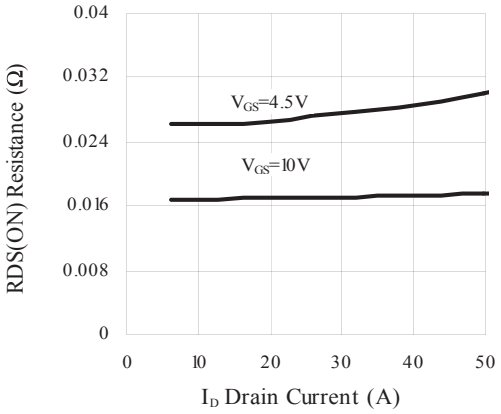


Figure 3. On-Resistance vs. Drain Current

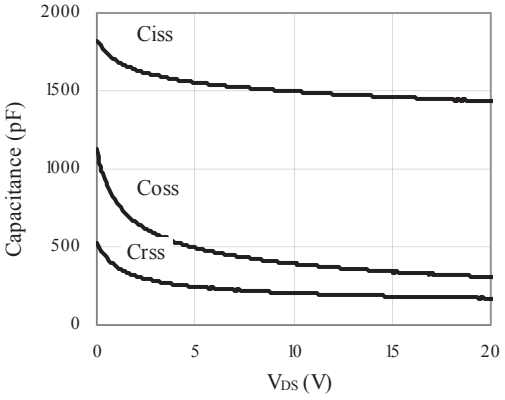


Figure 4. Capacitance

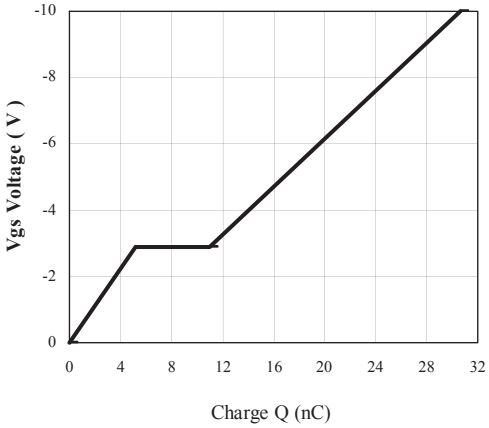


Figure 5. Gate Charge

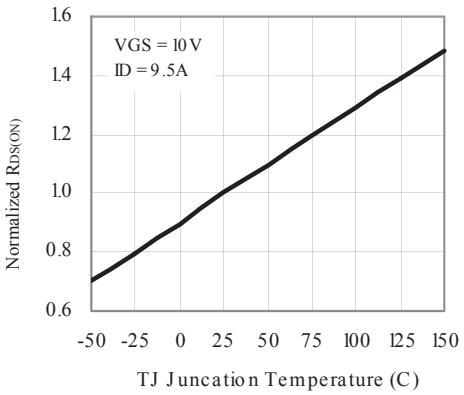


Figure 6. On-Resistance vs. Junction Temperature

Typical Electrical Characteristics (P-Channel)

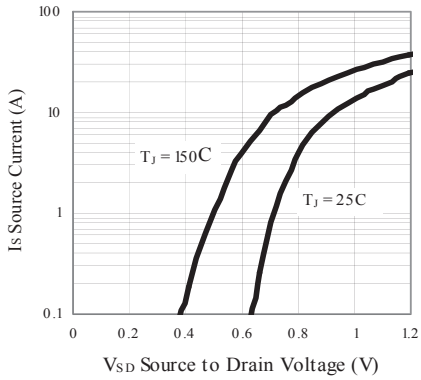


Figure 7. Source-Drain Diode Forward Voltage

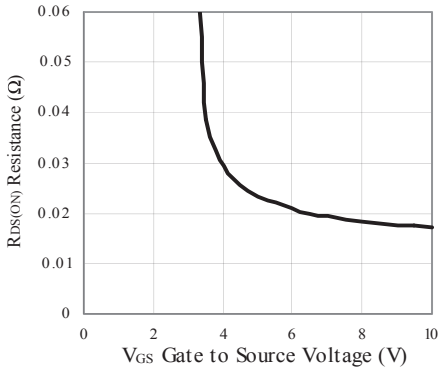


Figure 8. On-Resistance vs. Gate-to-Source Voltage

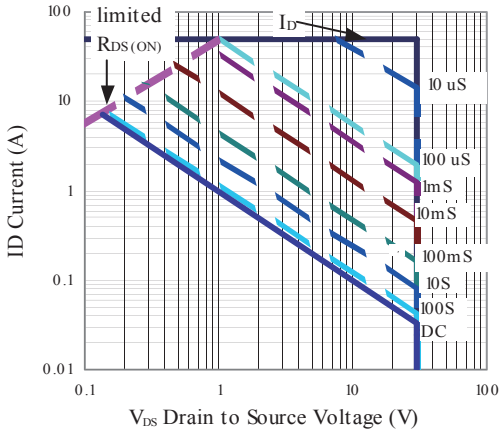


Figure 9. Maximum Safe Operating Area

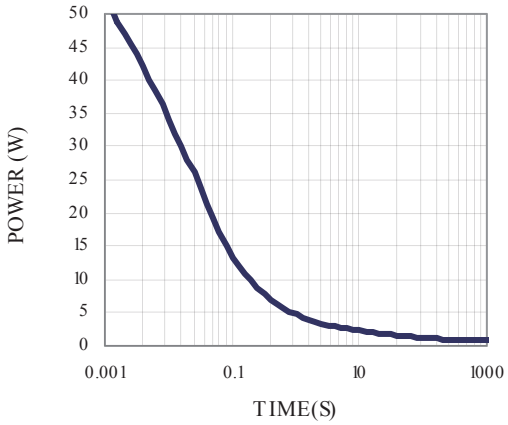


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

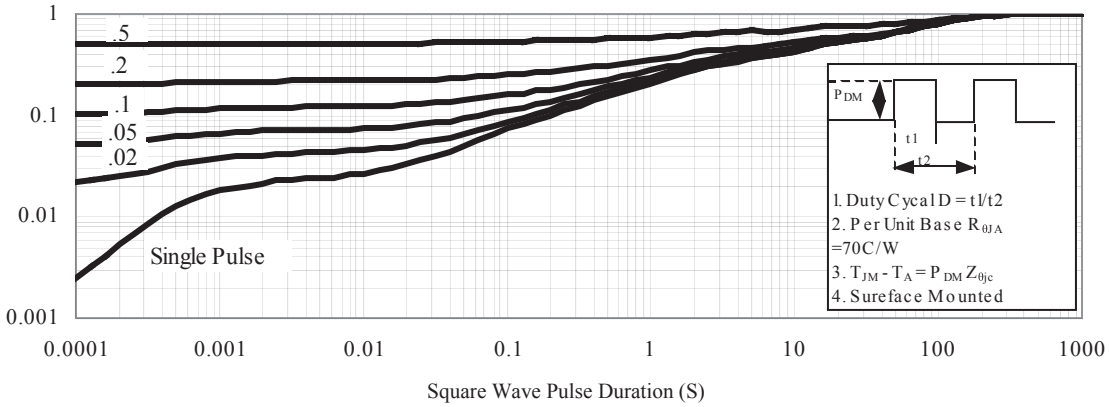
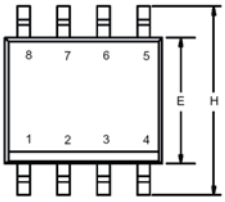
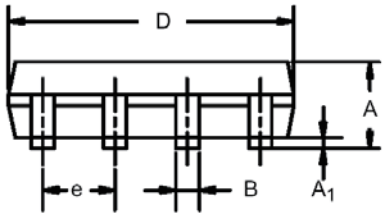


Figure 11. Transient Thermal Response Curve

Package Information

SO-8: 8LEAD





Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°