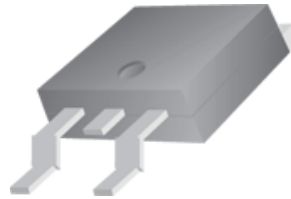


N-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications



PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
40	32 @ $V_{GS} = 10V$	33
	42 @ $V_{GS} = 4.5V$	29

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_C = 25^\circ\text{C}$	I_D	33	A
Pulsed Drain Current ^b		I_{DM}	40	
Continuous Source Current (Diode Conduction) ^a		I_S	30	A
Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	50.0	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

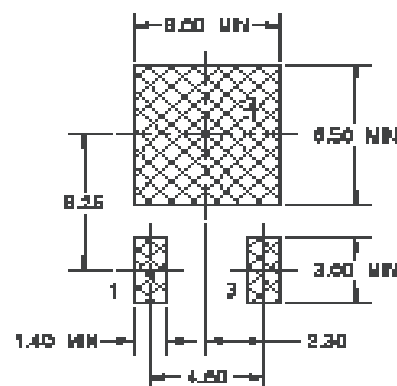
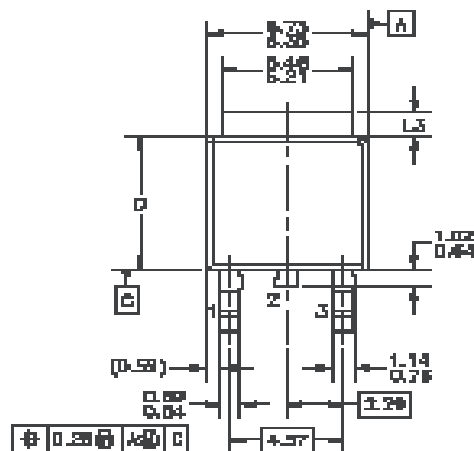
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	uA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	34			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 33 A			32	mΩ
		V _{GS} = 4.5 V, I _D = 29 A			42	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 33 A		22		S
Diode Forward Voltage	V _{SD}	I _S = 34 A, V _{GS} = 0 V		1.1		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 33 A		4.0		nC
Gate-Source Charge	Q _{gs}			1.1		
Gate-Drain Charge	Q _{gd}			1.4		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω , I _D = 34 A, V _{GEN} = 10 V		16		nS
Rise Time	t _r			5		
Turn-Off Delay Time	t _{d(off)}			23		
Fall-Time	t _f			3		

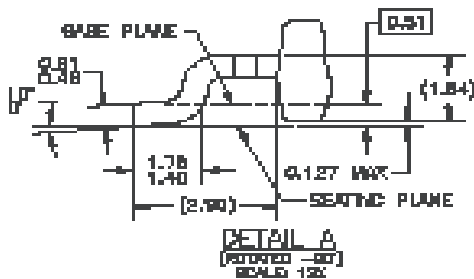
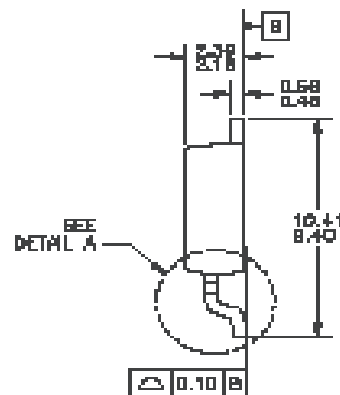
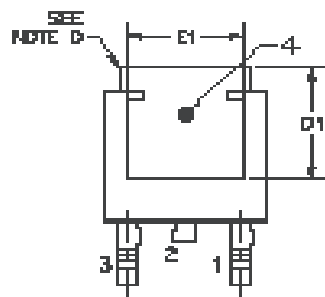
Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) THIS PACKAGE CONFORMS TO JEDEC, TO-263, ISSUE C, VARIATION AA, 30 DE, DATED NOV. 1999.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) DIMENSIONS L3, L4, E1 AND 1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.62-2.52
D	0.92-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.41 MIN	4.27 MIN