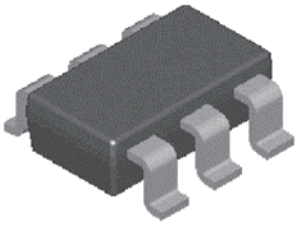
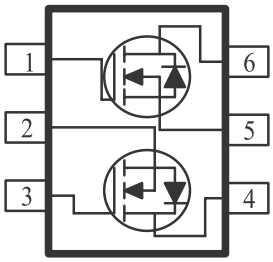
Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
20	0.047 @ V_{GS} = 4.5 V	4.1
	0.055 @ V_{GS} = 2.5V	3.8

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	4.1	A
	T_A=70°C		3.3	
Pulsed Drain Current[b]		I_{DM}	8	
Continuous Source Current (Diode Conduction)[a]		I_S	1.05	A
Power Dissipation[a]	T_A=25°C	P_D	1.15	W
	T_A=70°C		0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient[a]	t <= 10 sec	R_{thJA}	93	110	°C/W
	Steady State		130	150	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	0.4			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 8 V			1	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			0.1	uA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			1	uA
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	30			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.1 A			0.047	Ω
		V_{GS} = 2.5 V, I_D = 3.8 A			0.055	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 10 V, I_D = 4.1 A		10		S
Diode Forward Voltage[A]	V_{SD}	I_S = 1.05 A, V_{GS} = 0 V		0.80		S
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS}=10V, V_{GS}=4.5V, I_D=4.1A		7.5		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=10V, V_{GS}=4.5V, I_D=1A , R_{GEN}=15Ω		5		nS
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			13		
Fall-Time	t_f			7		

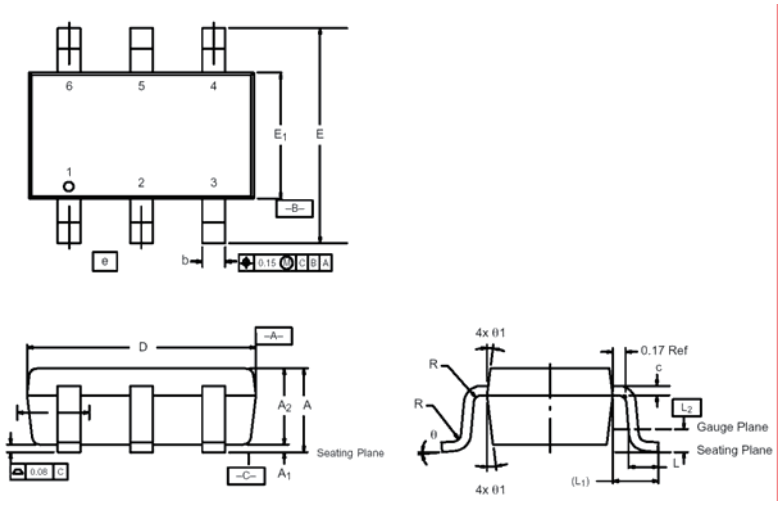
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

TSOP-6: 6LEAD



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	–	1.10	0.036	–	0.043
A_1	0.01	–	0.10	0.0004	–	0.004
A_2	0.84	–	1.00	0.033	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	1.00 BSC			0.0394 BSC		
L	0.35	–	0.50	0.014	–	0.020
L_1	0.60 Ref			0.024 Ref		
L_2	0.25 BSC			0.010 BSC		
R	0.10	–	–	0.004	–	–
θ	0°	4°	8°	0°	4°	8°
$θ_1$	7° Nom			7° Nom		