

N-Channel 150-V (D-S) MOSFET

Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

Typical Applications:

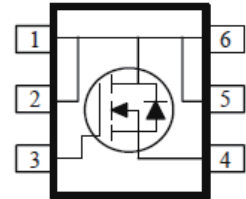
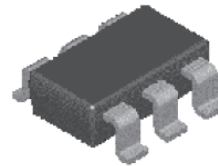
- PoE PSE and PD Circuits
- LED Inverter Circuits
- 48V-Input DC/DC Conversion Circuits

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
150	245 @ $V_{GS} = 10V$	2.4
	288 @ $V_{GS} = 4.5V$	2.2



RoHS
COMPLIANT
HALOGEN
FREE

TSOP-6



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	2.4	A
		1.9	
Pulsed Drain Current ^b	I_{DM}	8	
Continuous Source Current (Diode Conduction) ^a	I_S	2.6	A
Power Dissipation ^a	P_D	2	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
		110	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

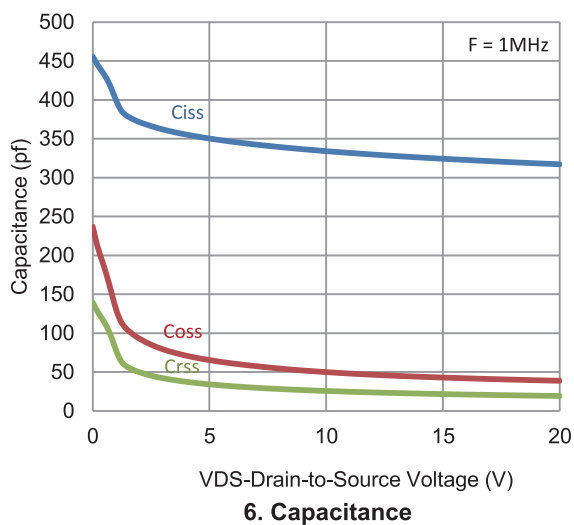
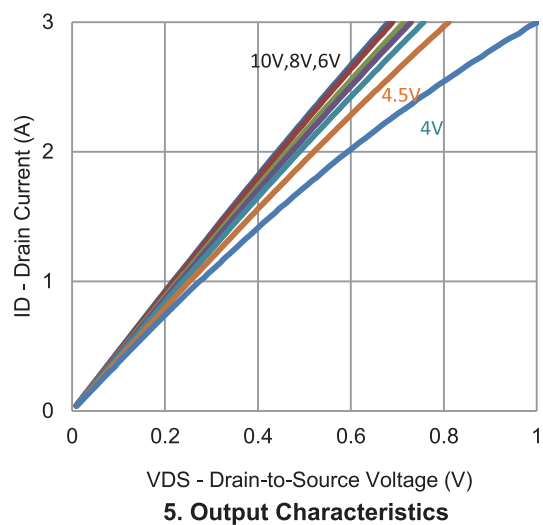
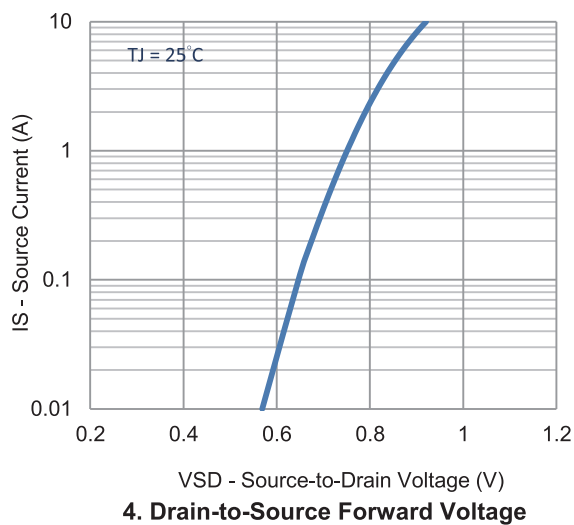
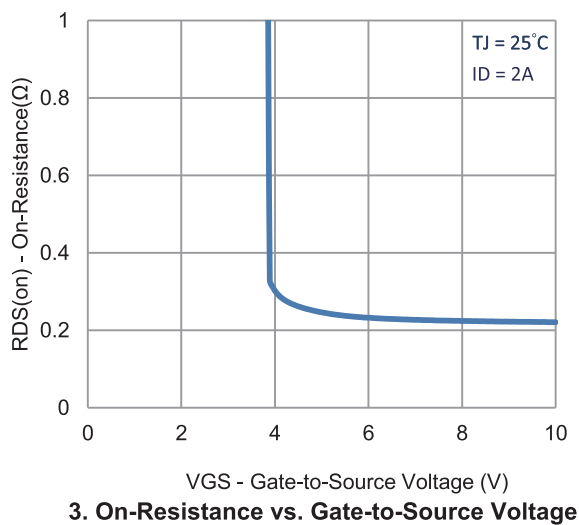
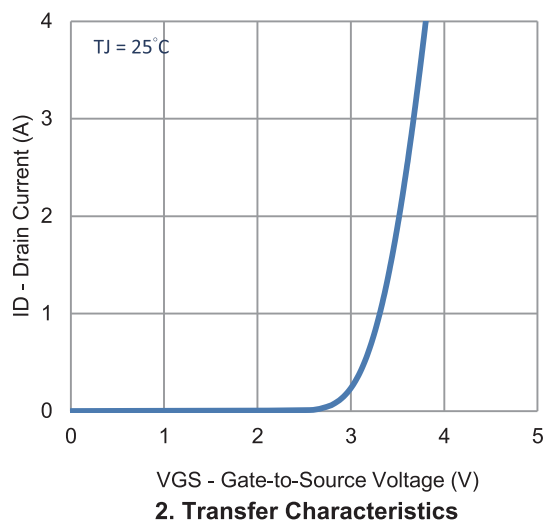
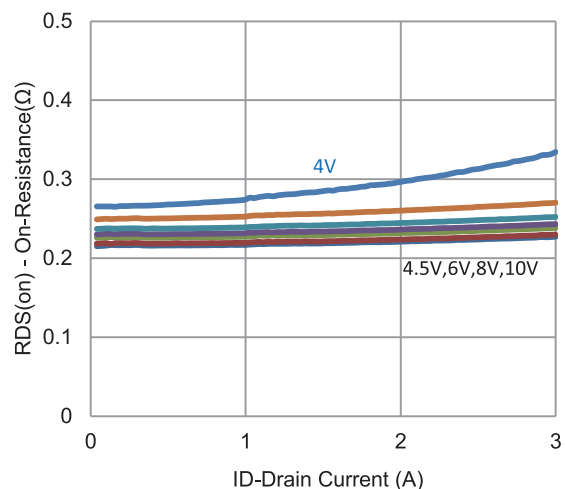
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 120 V, V_{GS} = 0 V$			1	μA
		$V_{DS} = 120 V, V_{GS} = 0 V, T_J = 55^\circ C$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	3.5			A
Drain-Source On-Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 2 A$			245	m Ω
		$V_{GS} = 4.5 V, I_D = 1.6 A$			288	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 V, I_D = 2 A$		8		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.3 A, V_{GS} = 0 V$		0.77		V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 75 V, V_{GS} = 4.5 V,$ $I_D = 2 A$		4		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			2.4		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 75 V, R_L = 37.5 \Omega,$ $I_D = 2 A,$ $V_{GEN} = 10 V, R_{GEN} = 6 \Omega$		4		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(off)}$			18		
Fall Time	t_f			7		
Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 Mhz$		324		pF
Output Capacitance	C_{oss}			42		
Reverse Transfer Capacitance	C_{rss}			21		

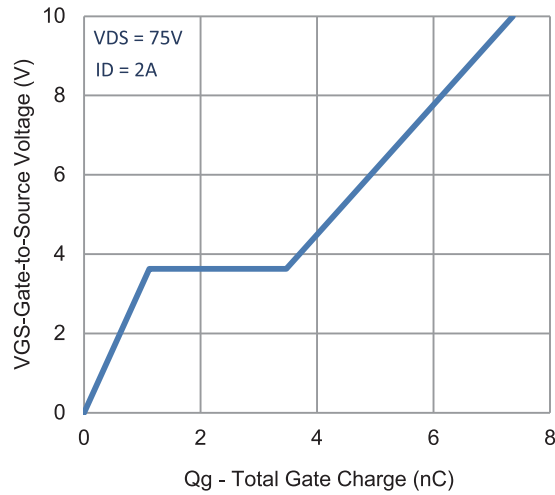
Notes

- a. Pulse test: PW $\leq$ 300us duty cycle $\leq$ 2%.
- b. Guaranteed by design, not subject to production testing.

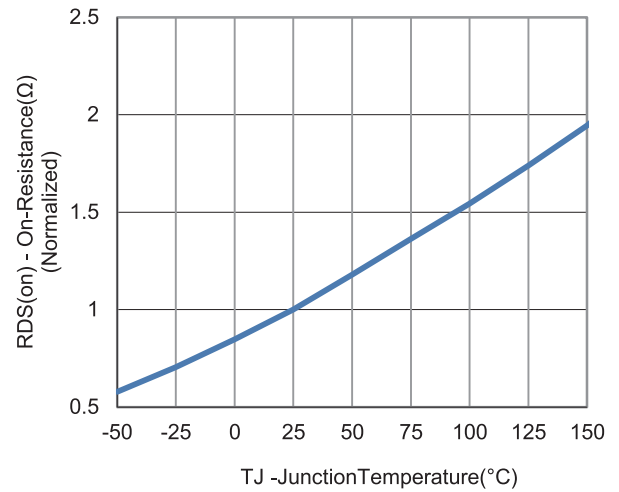
Typical Electrical Characteristics



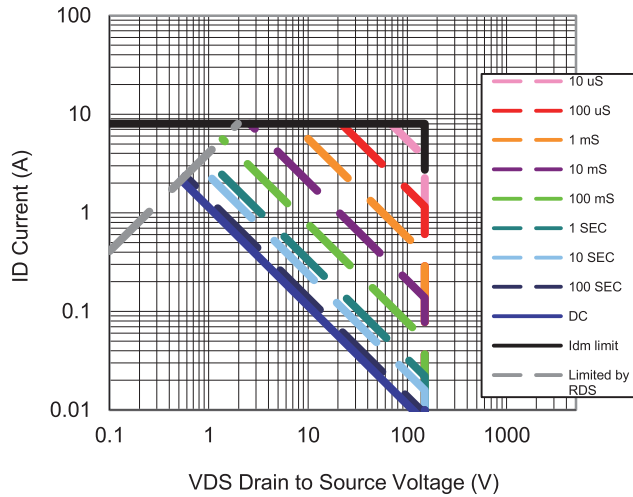
Typical Electrical Characteristics



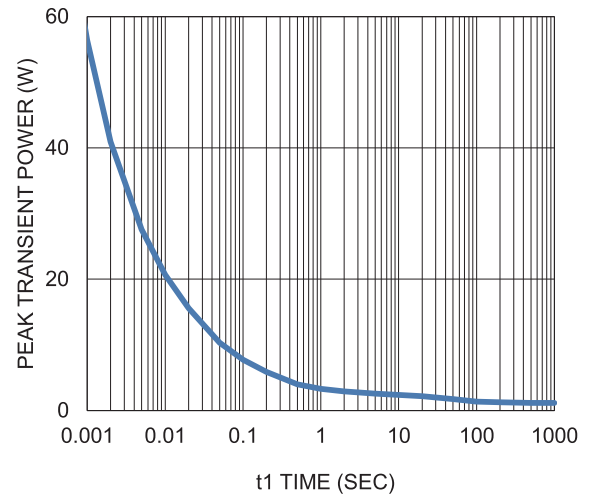
7. Gate Charge



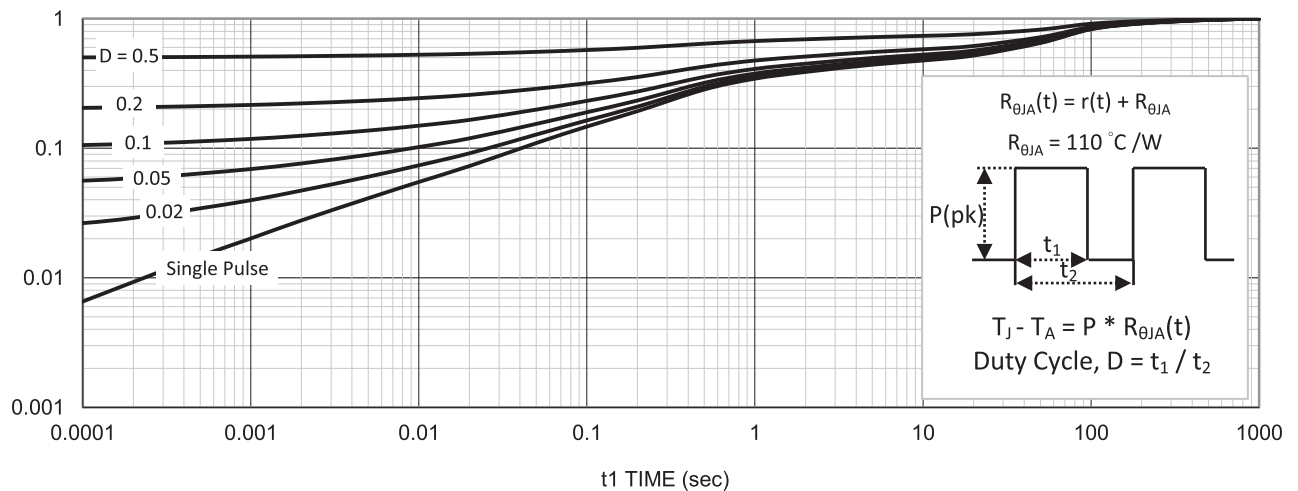
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

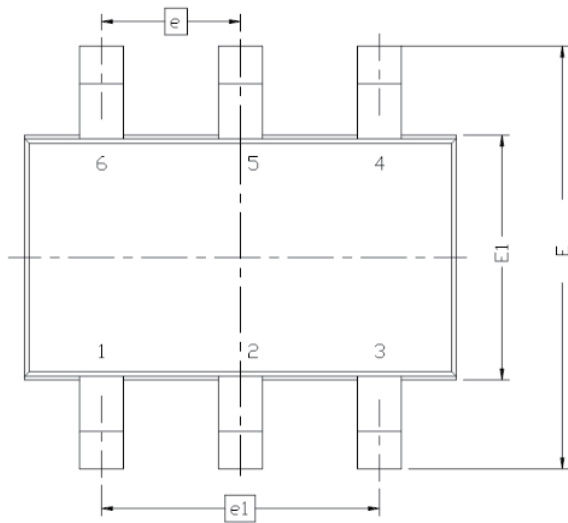


10. Single Pulse Maximum Power Dissipation

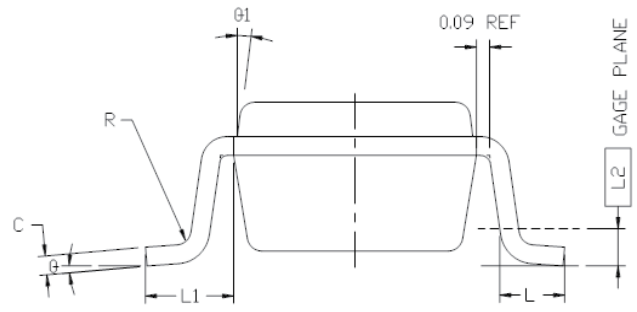
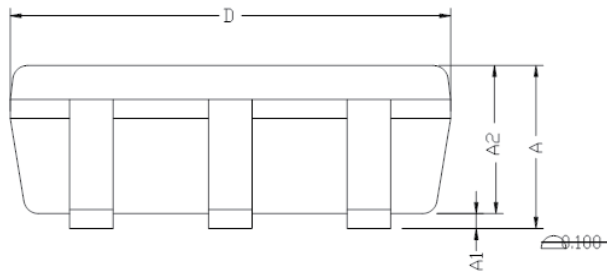


11. Normalized Thermal Transient Junction to Ambient

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	---	1.10
A1	0.01	---	0.10
A2	0.70	---	1.00
b	0.25	0.32	0.40
c	0.10	0.15	0.20
D	2.95	3.05	3.10
E	2.70	2.85	2.98
E1	1.55	1.65	1.70
e	0.95 BSC		
L	0.30	---	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7° NOM		



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.