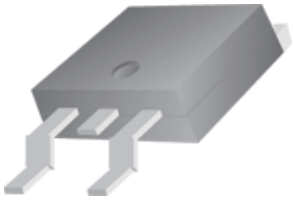
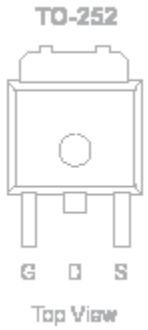
N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TO-252 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	59 @ V_{GS} = 4.5V	24
	88 @ V_{GS} = 2.5V	20





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current[a]	T_C=25°C	I_D	24	A
Pulsed Drain Current[b]		I_{DM}	40	
Continuous Source Current (Diode Conduction)[a]		I_S	30	A
Power Dissipation[a]	T_C=25°C	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

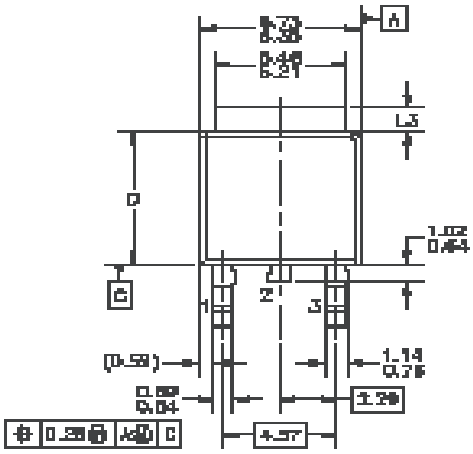
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	0.7			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	uA
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	34			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 12 A			59	mΩ
		V_{GS} = 2.5 V, I_D = 10 A			88	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 10 V, I_D = 12 A		22		S
Diode Forward Voltage	V_{SD}	I_S = 24 A, V_{GS} = 0 V		1.1		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 10 A		7.5		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.0		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 25 Ω , I_D = 24 A, V_{GEN} = 10 V		16		nS
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(off)}$			23		
Fall-Time	t_f			3		

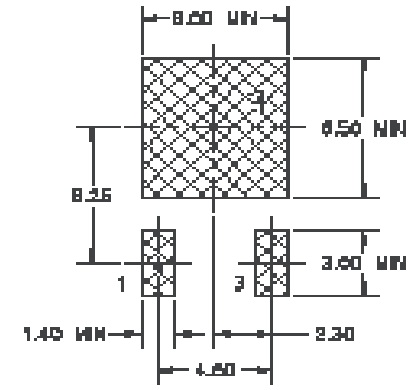
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

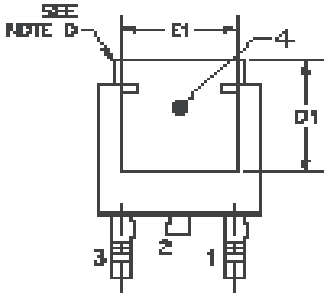
b. Guaranteed by design, not subject to production testing.

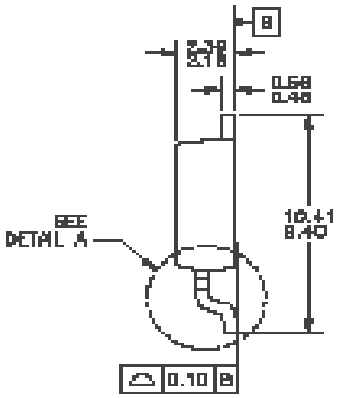
Package Information

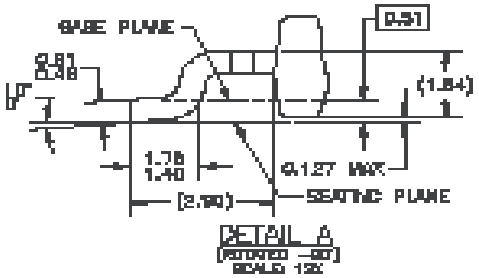




LAND PATTERN RECOMMENDATION







NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO-263, ISSUE C, VARIATION AA & AB, DATED NOV. 1989.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.508–1.27	1.60–2.60
D	8.40–8.80	8.40–8.80
E1	6.22 MIN	3.81 MIN
D1	5.21 MIN	4.37 MIN