

P-Channel 100-V (D-S) MOSFET

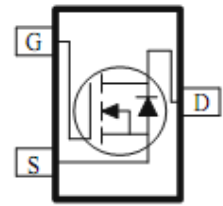
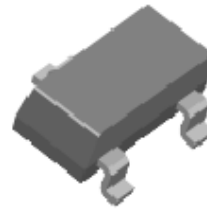
Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-100	1.2 @ $V_{GS} = -10V$	-1
	1.3 @ $V_{GS} = -4.5V$	-0.9



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-1	A
	$T_A = 70^\circ\text{C}$		-0.8	
Pulsed Drain Current ^b		I_{DM}	-10	
Continuous Source Current (Diode Conduction) ^a		I_S	-1.6	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.3	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady State		166	

Notes

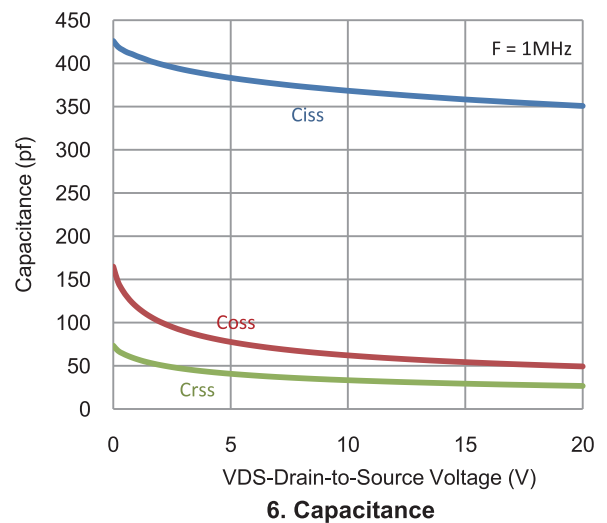
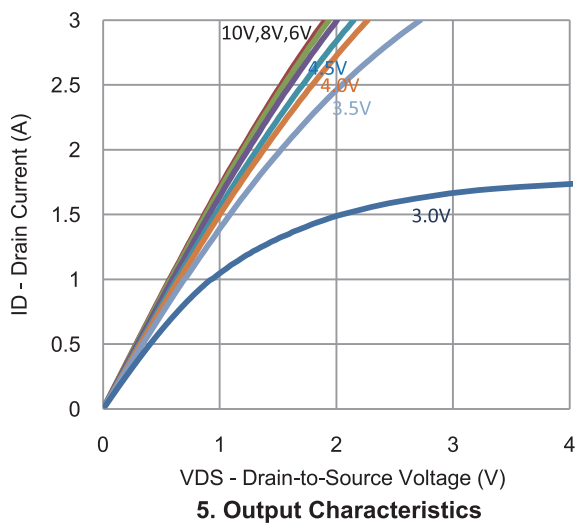
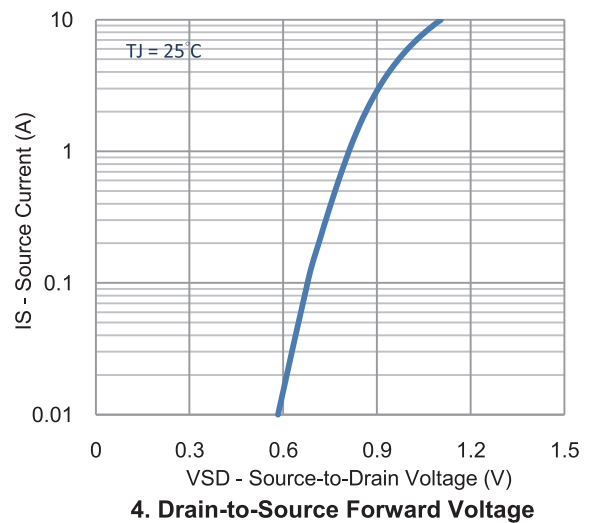
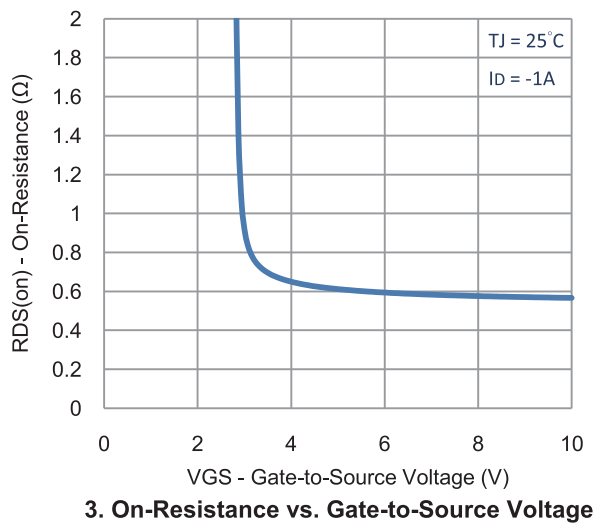
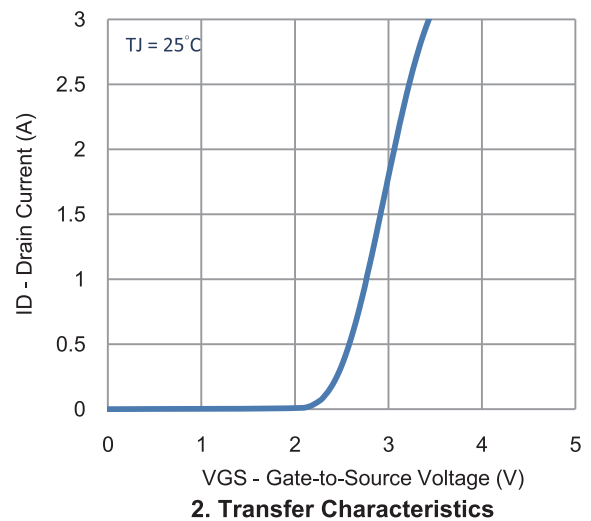
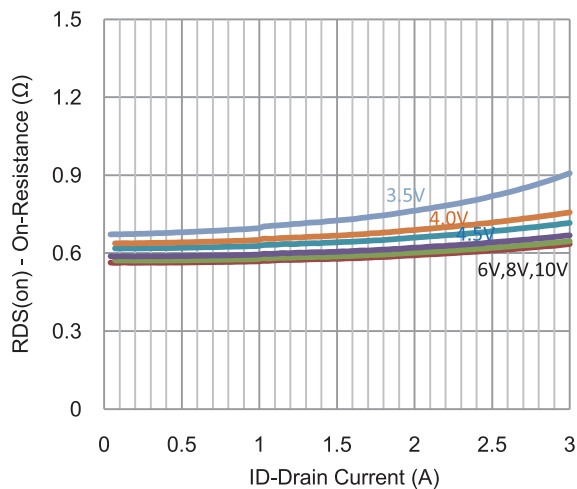
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	-1		-3.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80 V$, $V_{GS} = 0 V$			1	μA
		$V_{DS} = -80 V$, $V_{GS} = 0 V$, $T_J = 55^\circ C$			25	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -10 V$, $V_{GS} = -10 V$	-10			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = -10 V$, $I_D = -1 A$			1.2	Ω
		$V_{GS} = -4.5 V$, $I_D = -0.9 A$			1.3	
Forward Transconductance	g_{fs}	$V_{DS} = -15 V$, $I_D = -1 A$		5		S
Diode Forward Voltage	V_{SD}	$I_S = -0.8 A$, $V_{GS} = 0 V$		-0.81		V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = -50 V$, $V_{GS} = -4.5 V$, $I_D = -1 A$		3.7		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50 V$, $R_L = 50 \Omega$, $I_D = -1 A$, $V_{GEN} = -10 V$, $R_{GEN} = 6 \Omega$		3.5		nS
Rise Time	t_r			3.8		
Turn-Off Delay Time	$t_{d(off)}$			15.5		
Fall-Time	t_f			10.3		
Input Capacitance	C_{iss}	$V_{DS} = -15 V$, $V_{GS} = 0 V$, $f = 1 MHz$		358		pF
Output Capacitance	C_{oss}			54		
Reverse Transfer Capacitance	C_{rss}			29		

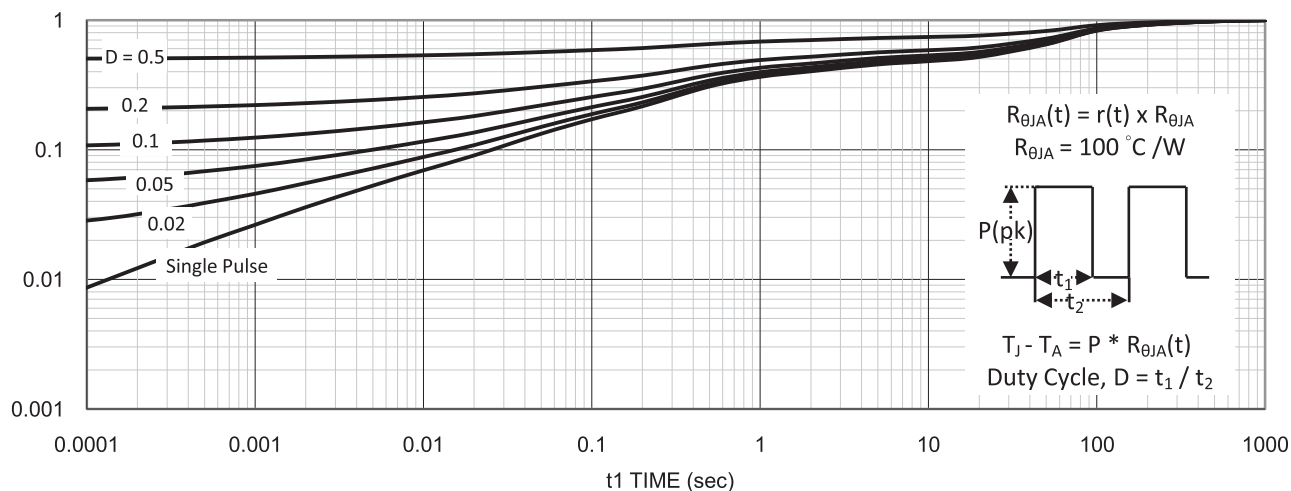
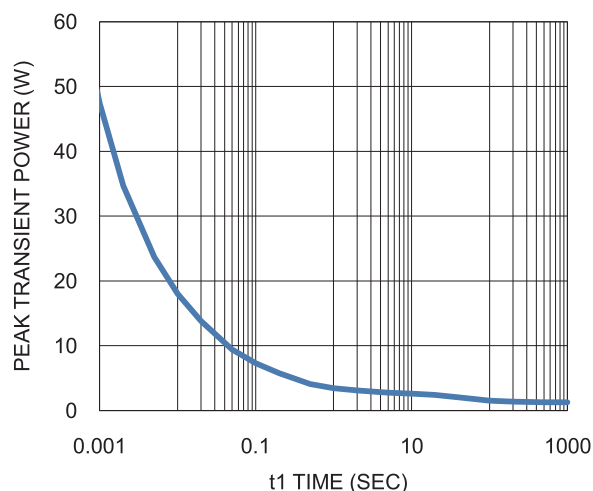
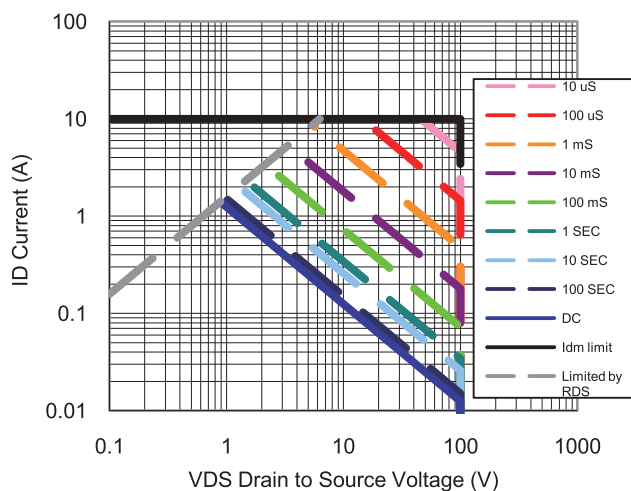
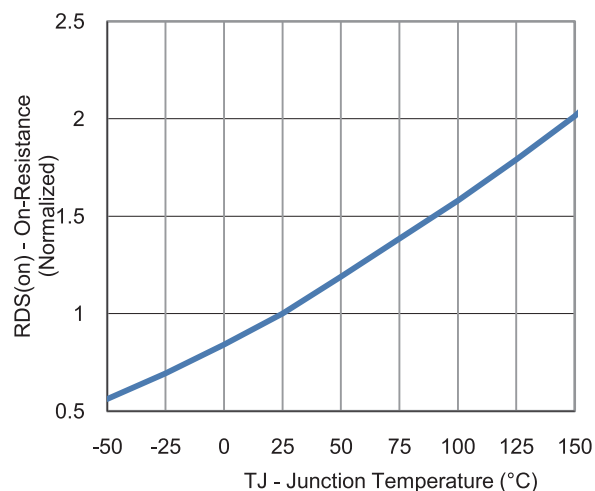
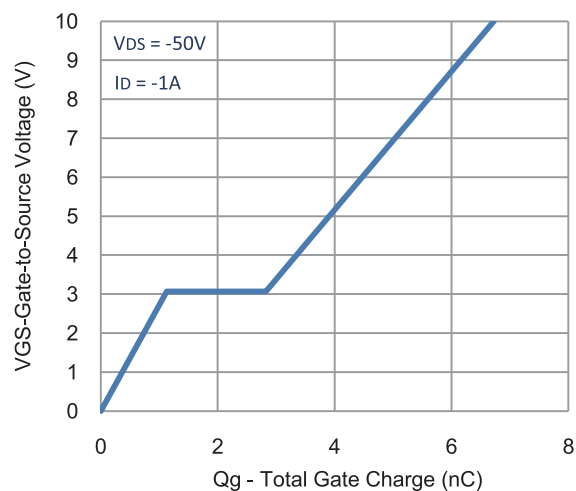
Notes

- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

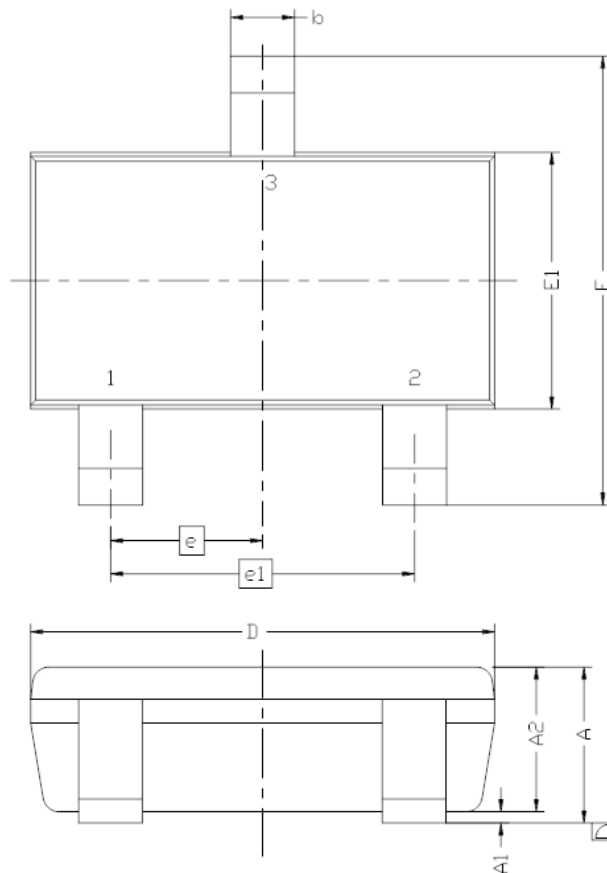
Typical Electrical Characteristics



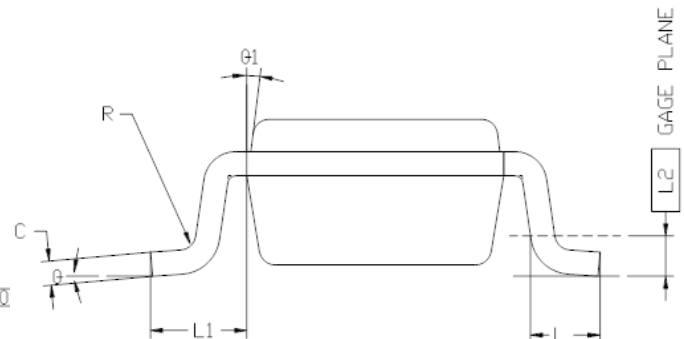
Typical Electrical Characteristics



Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM		



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.
5. Dimension "B" Does Not Include Dambar Protrusion. Allowable Dambar Protrusion Shall Be 0.08 mm Total In Excess Of "B" Dimension At Maximum Material Condition. The Dambar Cannot Be Located On The Lower Radius Of The Foot.