

P-Channel 200-V (D-S) MOSFET

Key Features:

- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed

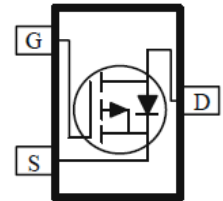
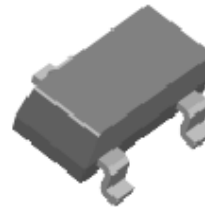
Typical Applications:

- PoE Power Sourcing Equipment
- PoE Powered Devices
- Telecom DC/DC converters
- White LED boost converters



RoHS
COMPLIANT
HALOGEN
FREE

SOT-23



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-200	2.5 @ $V_{GS} = -10V$	-0.6
	2.8 @ $V_{GS} = -5.5V$	-0.5

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	-0.6	A
	$T_A = 70^\circ\text{C}$		-0.5	
Pulsed Drain Current ^b		I_{DM}	5	
Continuous Source Current (Diode Conduction) ^a		I_S	1.2	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.3	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady State		166	

Notes

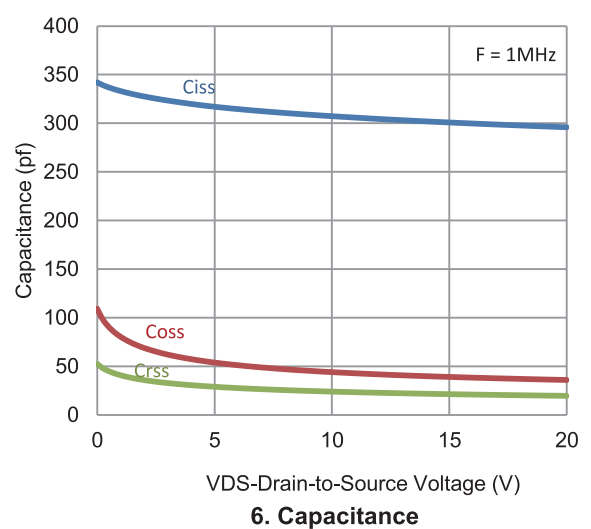
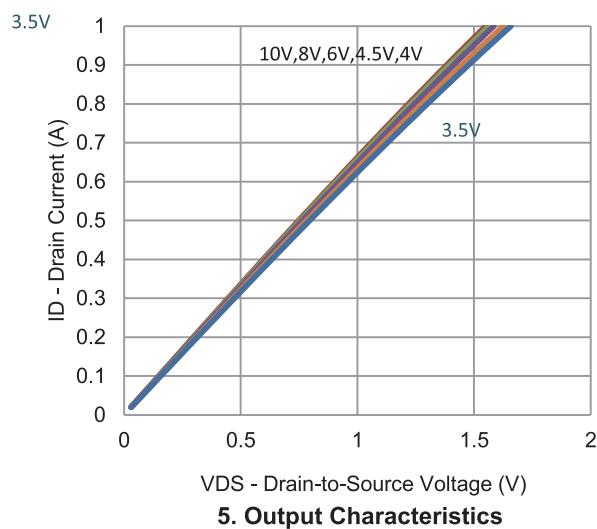
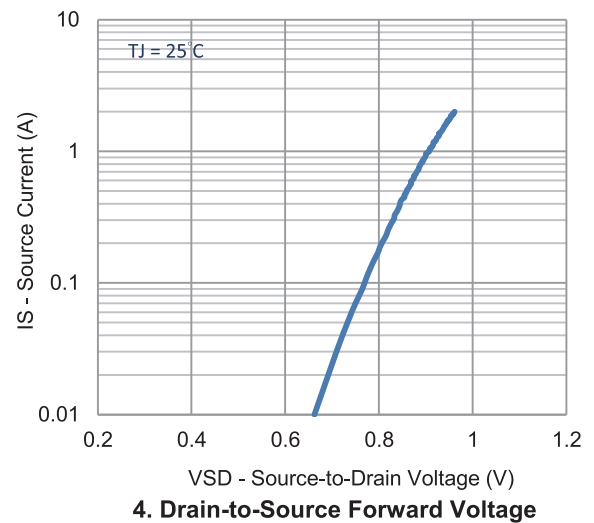
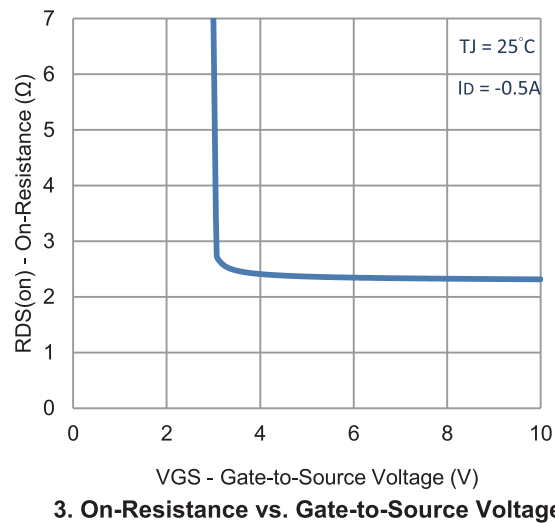
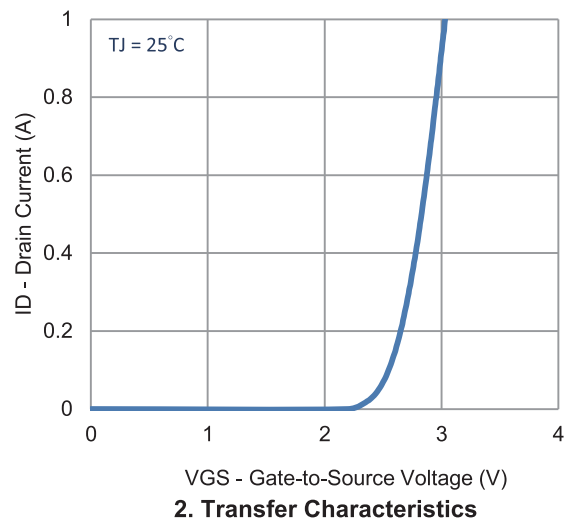
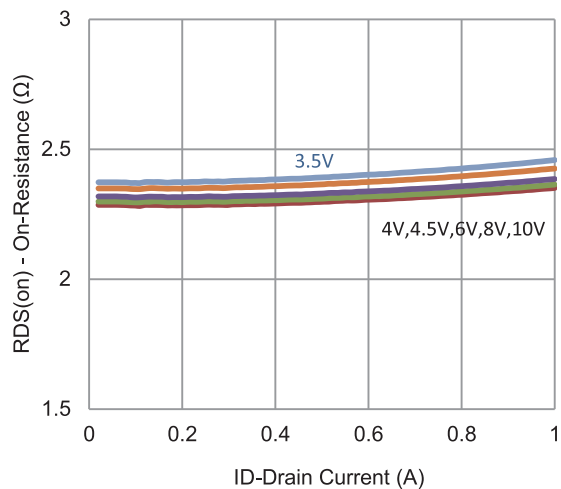
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -160 V, V_{GS} = 0 V$			-1	μA
		$V_{DS} = -160 V, V_{GS} = 0 V, T_J = 55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS} = -5 V, V_{GS} = -10 V$	-0.5			A
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = -10 V, I_D = -0.5 A$			2.5	Ω
		$V_{GS} = -5.5 V, I_D = -0.4 A$			2.8	
Forward Transconductance	g_{fs}	$V_{DS} = -15 V, I_D = -0.5 A$		1.8		S
Diode Forward Voltage	V_{SD}	$I_S = -0.6 A, V_{GS} = 0 V$		-0.87		V
Dynamic						
Total Gate Charge	Q_g	$V_{DS} = -100 V, V_{GS} = -5.5 V,$ $I_D = -0.5 A$		3.7		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -100 V, R_L = 200 \Omega,$ $I_D = -0.5 A,$ $V_{GEN} = -10 V, R_{GEN} = 6 \Omega$		4		ns
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			13		
Fall-Time	t_f			10		
Input Capacitance	C_{iss}	$V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz$		301		pF
Output Capacitance	C_{oss}			39		
Reverse Transfer Capacitance	C_{rss}			21		

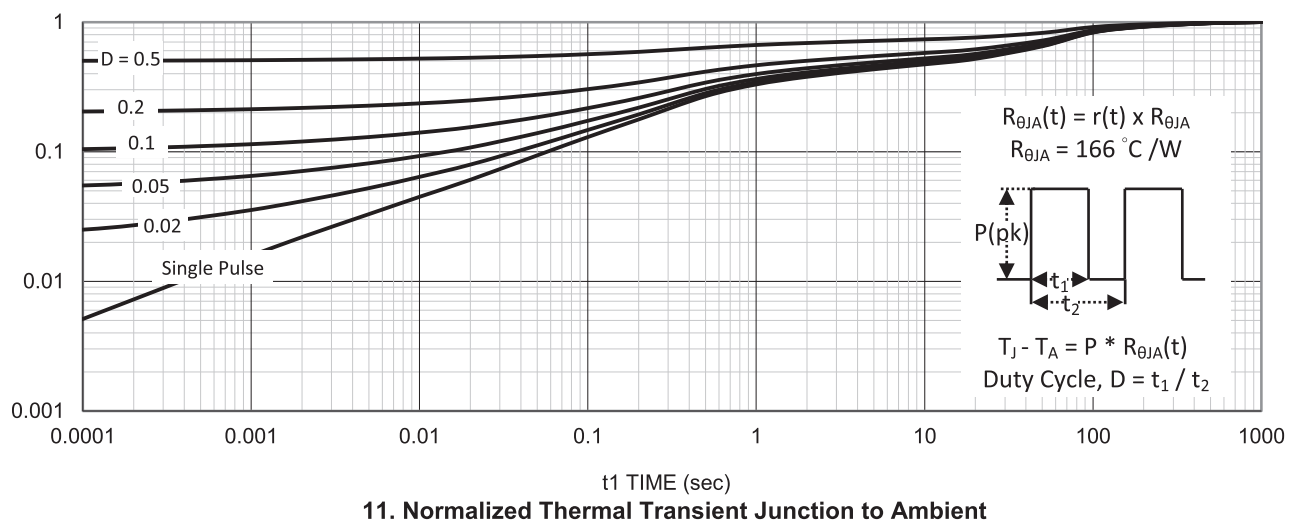
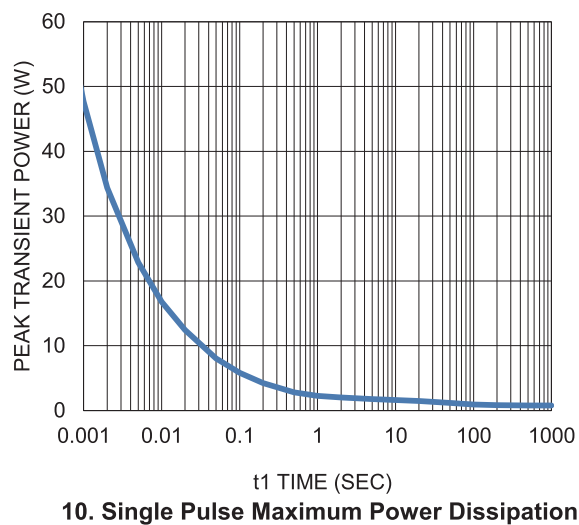
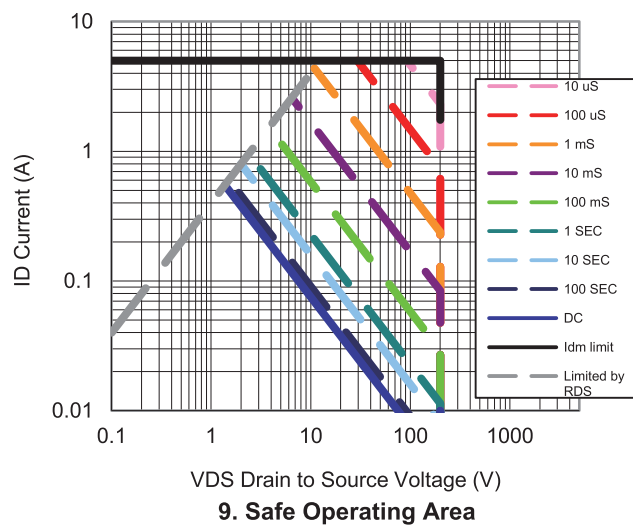
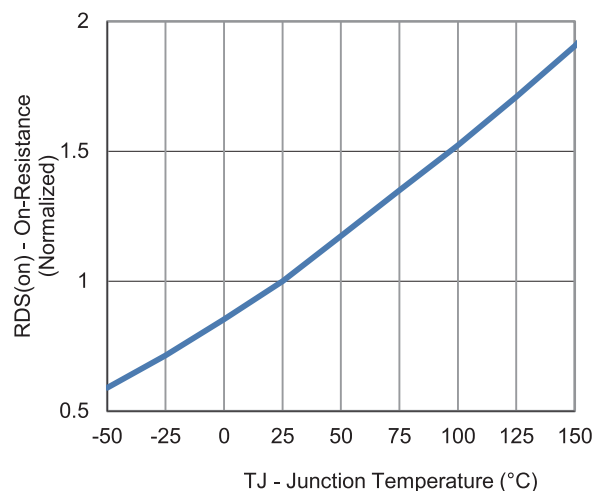
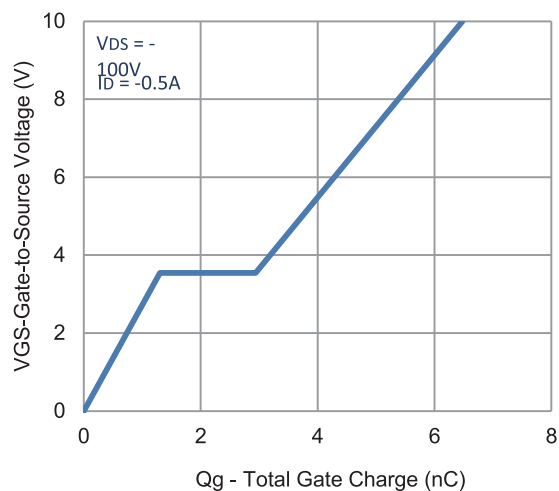
Notes

- Pulse test: PW $\leq 300 \mu s$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

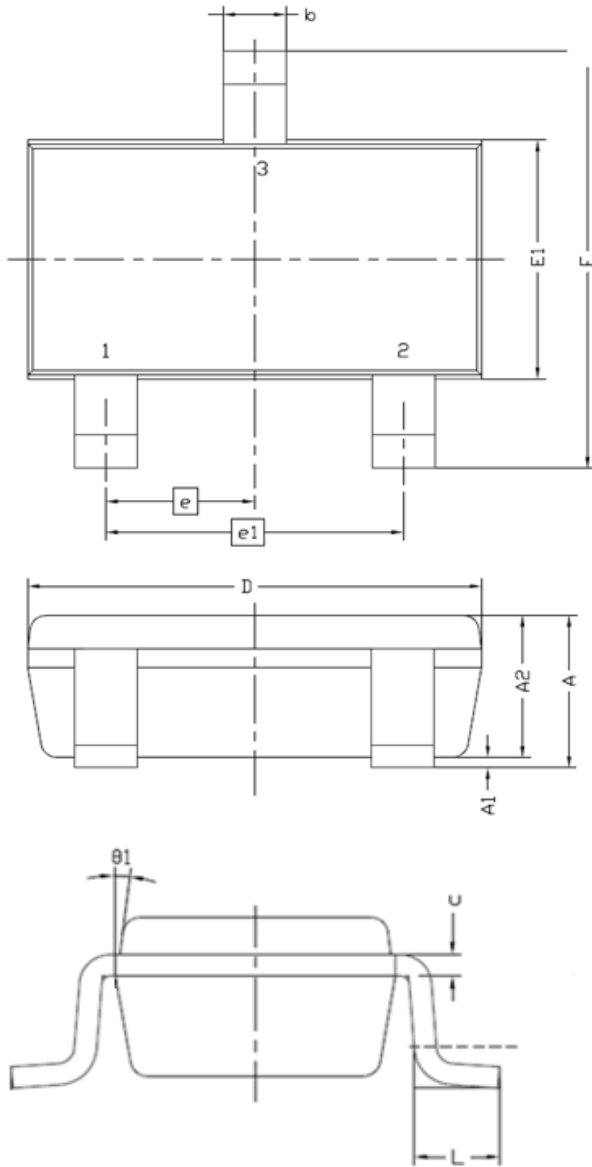
Typical Electrical Characteristics



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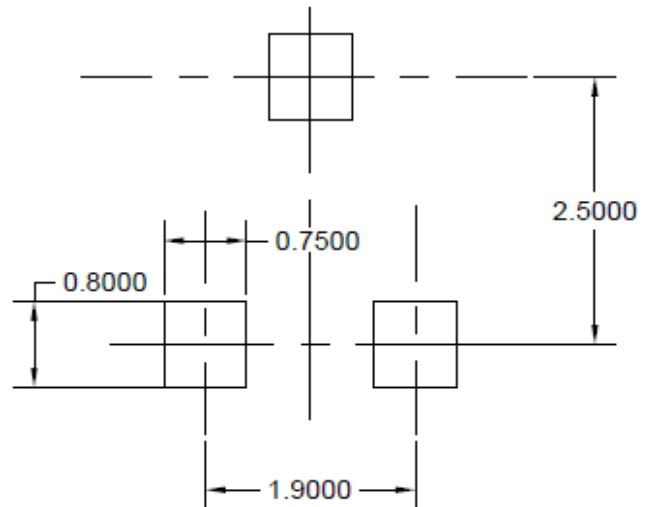


Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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