

## N-Channel 40-V (D-S) MOSFET

### Key Features:

- Low  $r_{DS(on)}$  trench technology
- Low thermal impedance
- Fast switching speed

### Typical Applications:

- Power Routing
- Li Ion Battery Packs
- Level Shifting and Driver Circuits

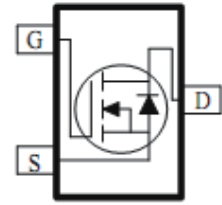
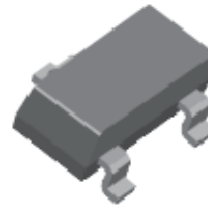
### PRODUCT SUMMARY

$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
40	26 @ $V_{GS} = 10V$	5.8
	35 @ $V_{GS} = 4.5V$	5.0

SOT-23



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>a</sup>	$I_D$	5.8	A
		4.6	
Pulsed Drain Current <sup>b</sup>	$I_{DM}$	30	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.1	A
Power Dissipation <sup>a</sup>	$P_D$	1.3	W
		0.8	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	100	$^\circ\text{C/W}$
		166	

### Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

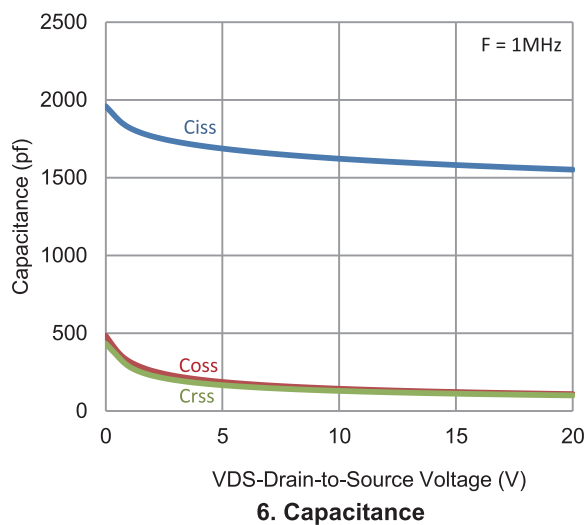
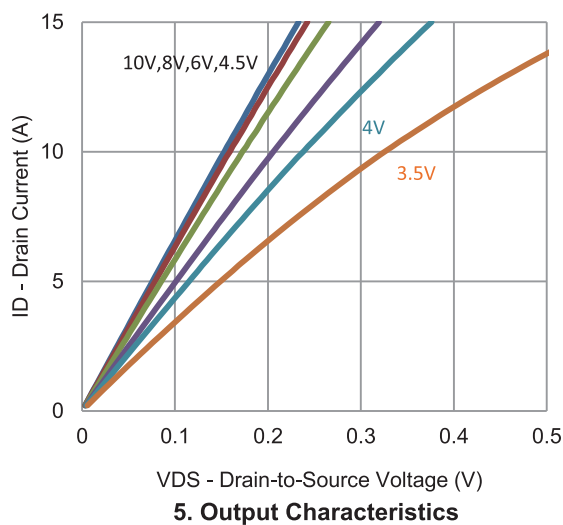
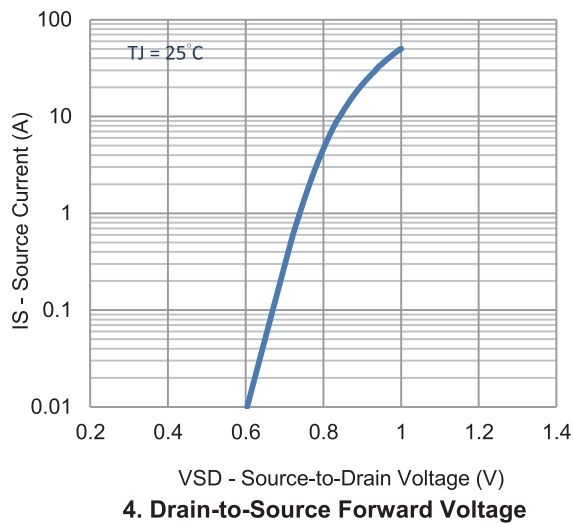
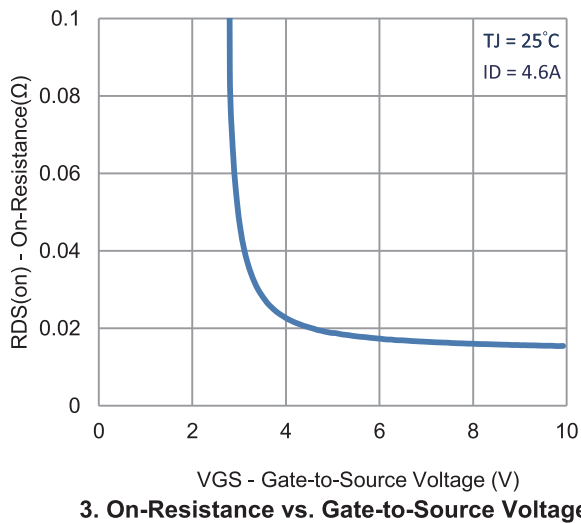
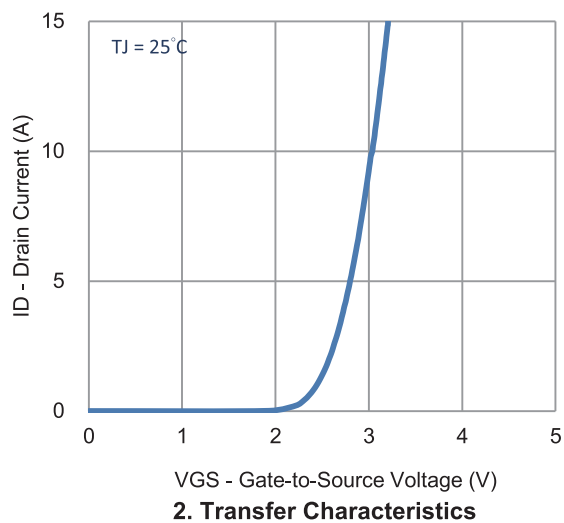
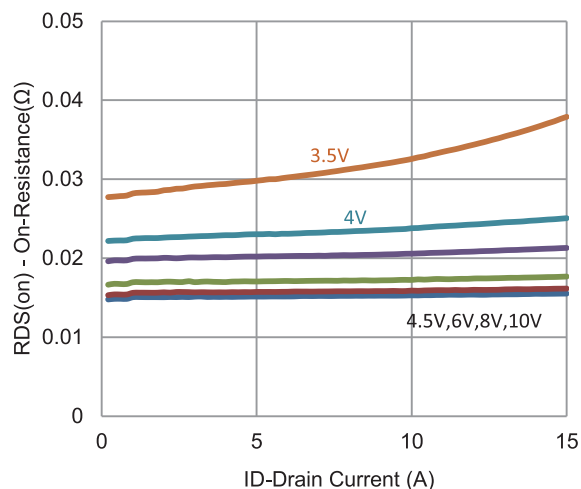
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 32 V, V_{GS} = 0 V$			1	$\mu A$
		$V_{DS} = 32 V, V_{GS} = 0 V, T_J = 55^\circ C$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5 V, V_{GS} = 10 V$	9			A
Drain-Source On-Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10 V, I_D = 4.6 A$			26	m $\Omega$
		$V_{GS} = 4.5 V, I_D = 3.7 A$			35	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 V, I_D = 4.6 A$		8		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1.1 A, V_{GS} = 0 V$		0.74		V
<b>Dynamic <sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 20 V, V_{GS} = 4.5 V,$ $I_D = 4.6 A$		9.9		nC
Gate-Source Charge	$Q_{gs}$			2.9		
Gate-Drain Charge	$Q_{gd}$			3.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS} = 20 V, R_L = 4.4 \Omega,$ $I_D = 4.6 A,$ $V_{GEN} = 10 V, R_{GEN} = 6 \Omega$		8		ns
Rise Time	$t_r$			5		
Turn-Off Delay Time	$t_{d(off)}$			32		
Fall Time	$t_f$			8		
Input Capacitance	$C_{iss}$	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1 Mhz$		1581		pF
Output Capacitance	$C_{oss}$			121		
Reverse Transfer Capacitance	$C_{rss}$			111		

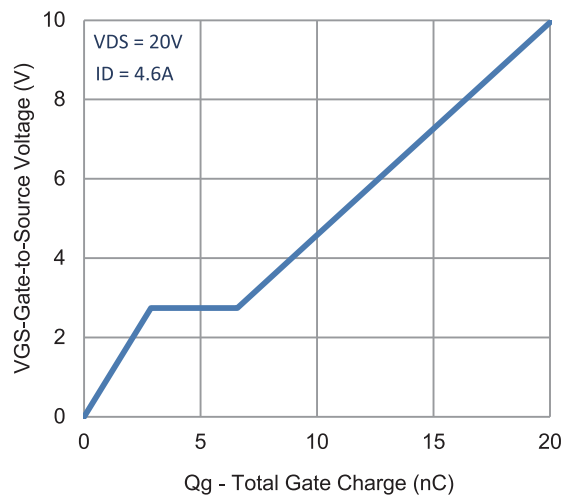
## Notes

- a. Pulse test: PW  $\leq$  300us duty cycle  $\leq$  2%.
- b. Guaranteed by design, not subject to production testing.

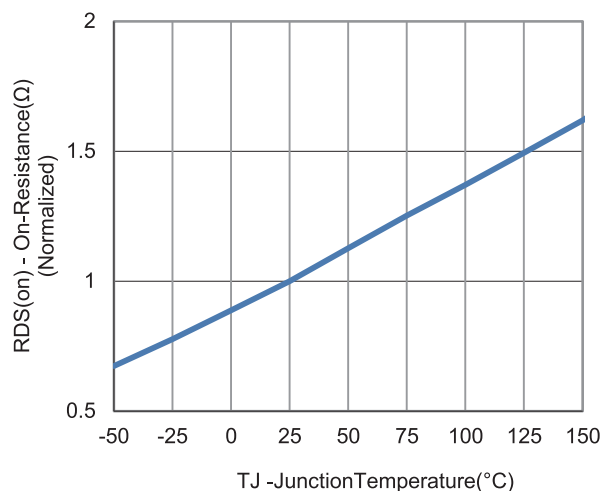
## Typical Electrical Characteristics



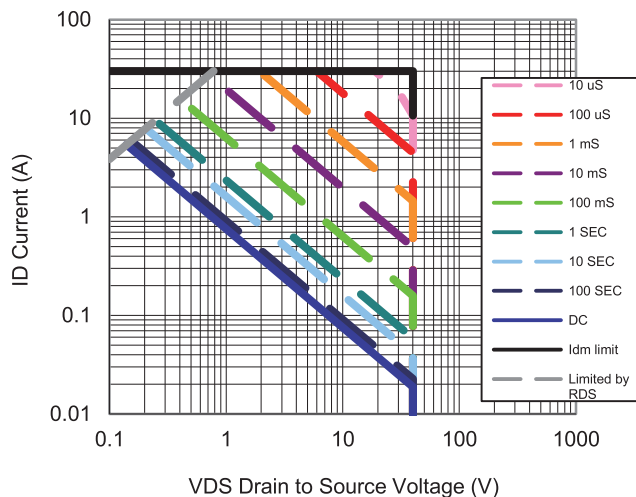
## Typical Electrical Characteristics



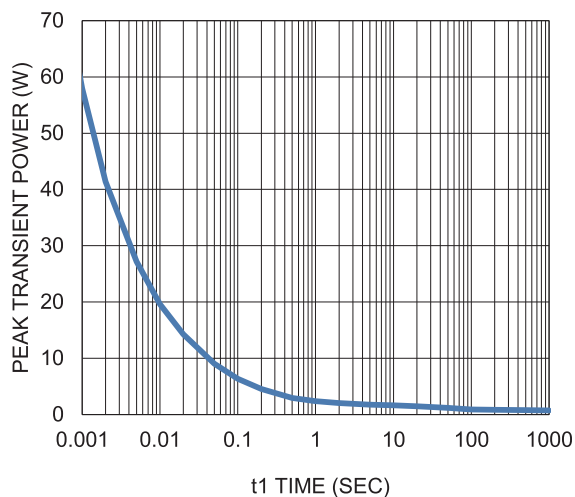
7. Gate Charge



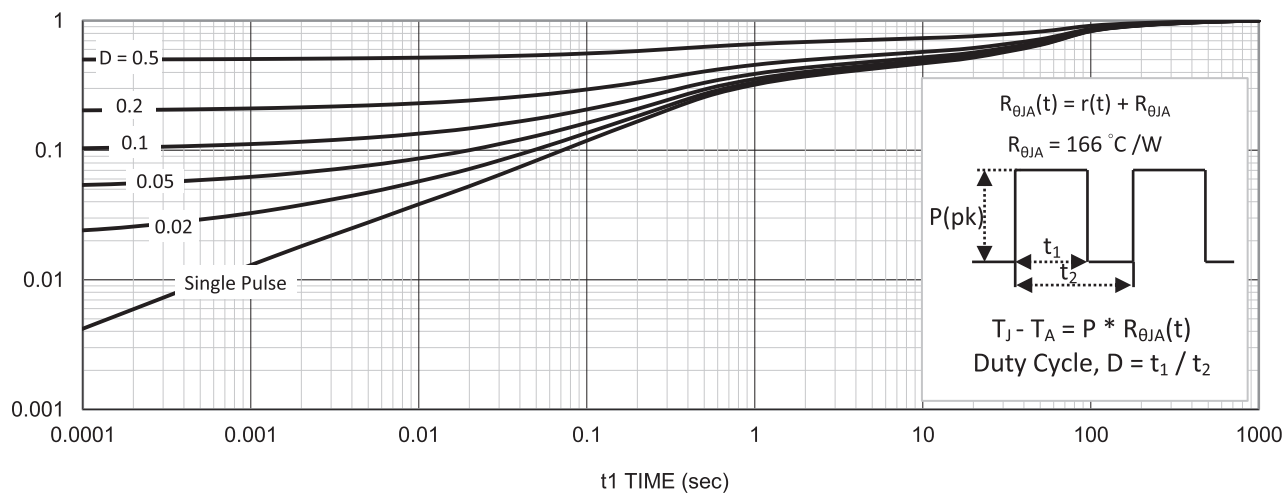
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

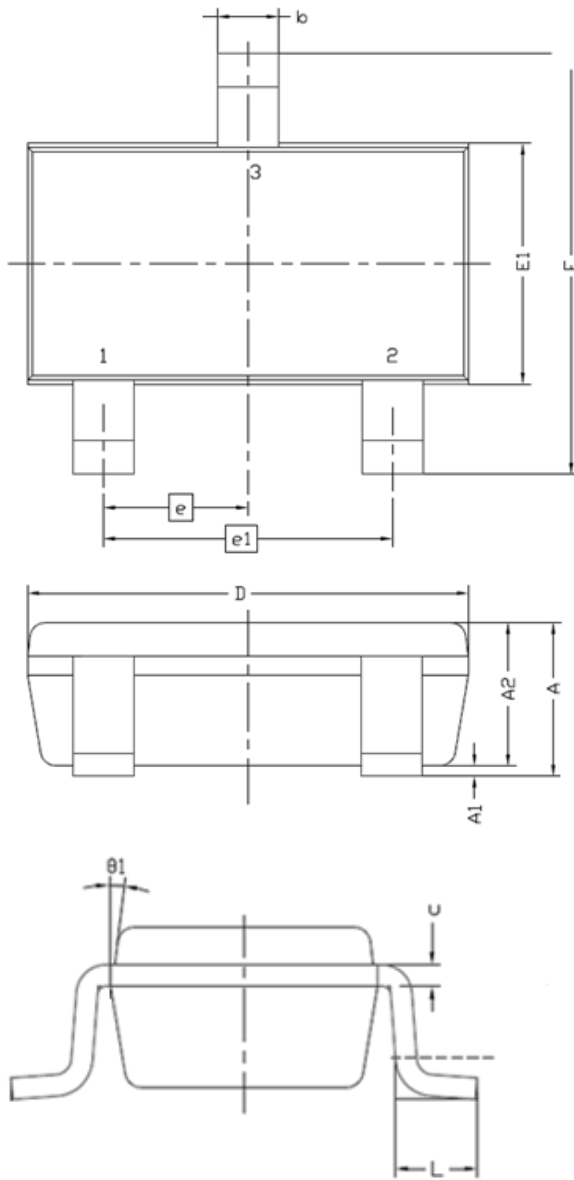


10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient

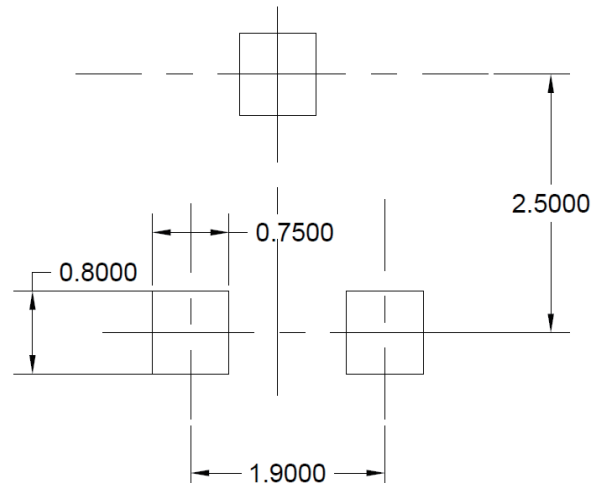
## Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

### Recommended Pad Layout

Note: Drain opening is recommended to be solder mask defined in a copper fill to provide improved thermal performance



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