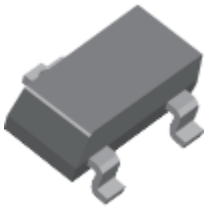
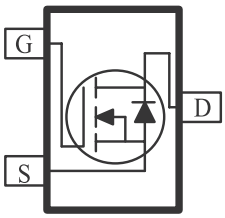
N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOT-23 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.085 @ V_{GS} = 10V	2.5
	0.125 @ V_{GS} = 4.5V	1.7





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	2.5	A
	T_A=70°C		2	
Pulsed Drain Current[b]		I_{DM}	10	
Continuous Source Current (Diode Conduction)[a]		I_S	0.46	A
Power Dissipation[a]	T_A=25°C	P_D	1.25	W
	T_A=70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 5 sec	R_{THJA}	150	°C/W
	Steady-State		200	

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 uA	1.0	1.5	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 8 V		4	100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V		7	1	uA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55°C			10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	6			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 2.5 A		62	85	mΩ
		V_{GS} = 4.5 V, I_D = 1.7 A		102	125	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 5 V, I_D = 3.0 A		3.5		S
Diode Forward Voltage	V_{SD}	I_S = 0.46 A, V_{GS} = 0 V		0.65		V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 2.5 A		3.5	7	nC
Gate-Source Charge	Q_{gs}			0.8	2	
Gate-Drain Charge	Q_{gd}			1.0	2	
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		720	1500	pF
Output Capacitance	C_{oss}			165	400	
Reverse Transfer Capacitance	C_{rss}			60	200	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, I_D = 1 A, R_G = 6 Ω, V_{GEN} = 4.5 V		10	20	ns
Rise Time	t_r			13	30	
Turn-Off Delay Time	$t_{d(off)}$			14	30	
Fall-Time	t_f			4	20	

Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics

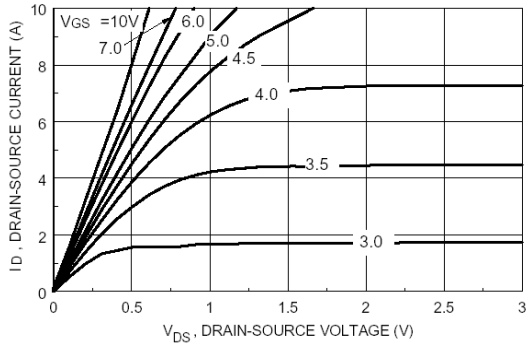


Figure 1. On-Region Characteristics

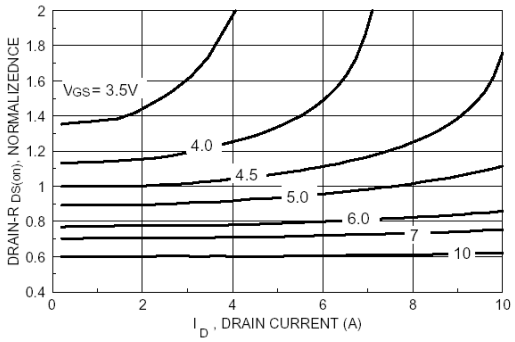


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

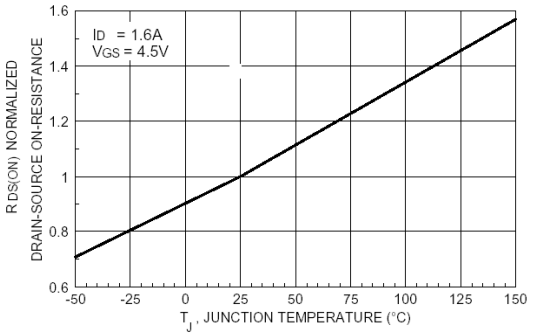


Figure 3. On-Resistance Variation with Temperature

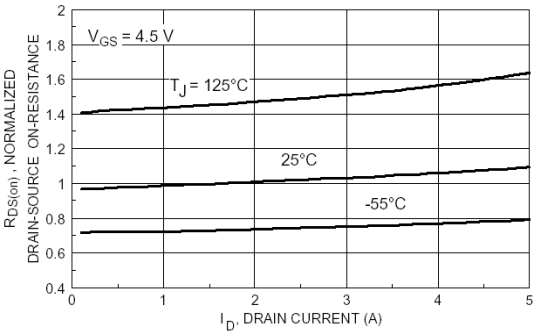


Figure 4. On-Resistance Variation with Drain Current and Temperature

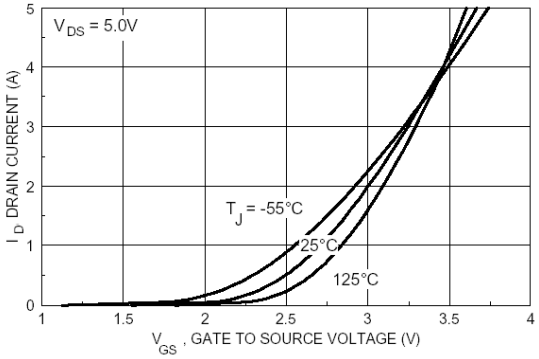


Figure 5. Transfer Characteristics

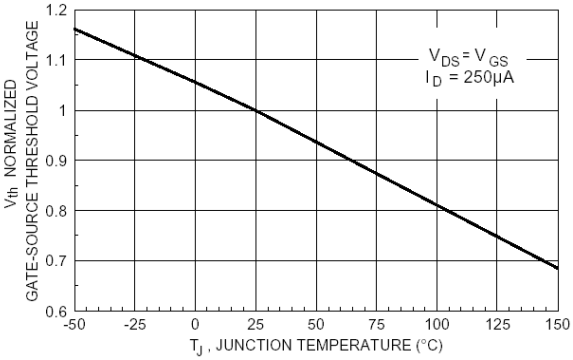


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics

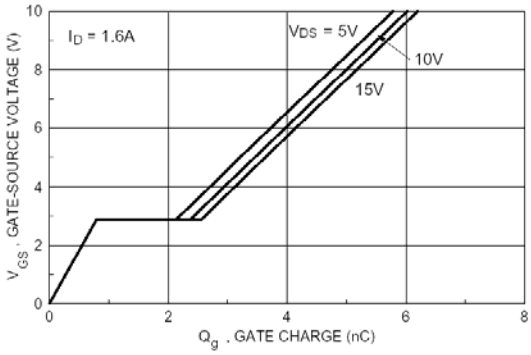


Figure 7. Gate Charge Characteristic

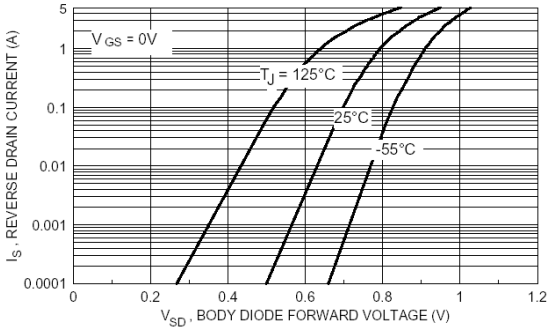


Figure 8. Capacitance Characteristic

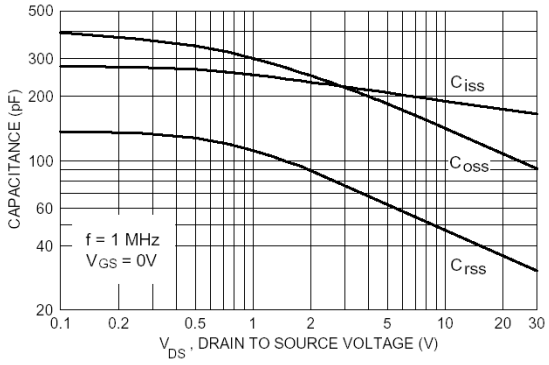


Figure 9. Maximum Safe Operating Area

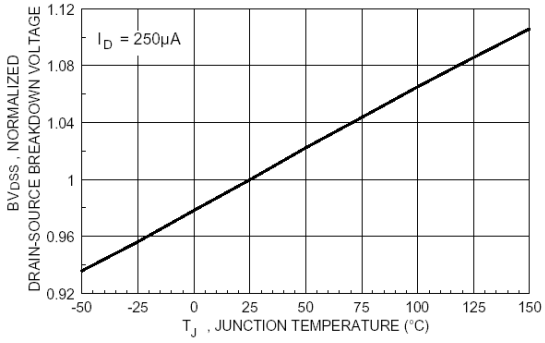


Figure 10. Breakdown Voltage Variation with Temperature

Normalized Thermal Transient Impedance, Junction to Ambient

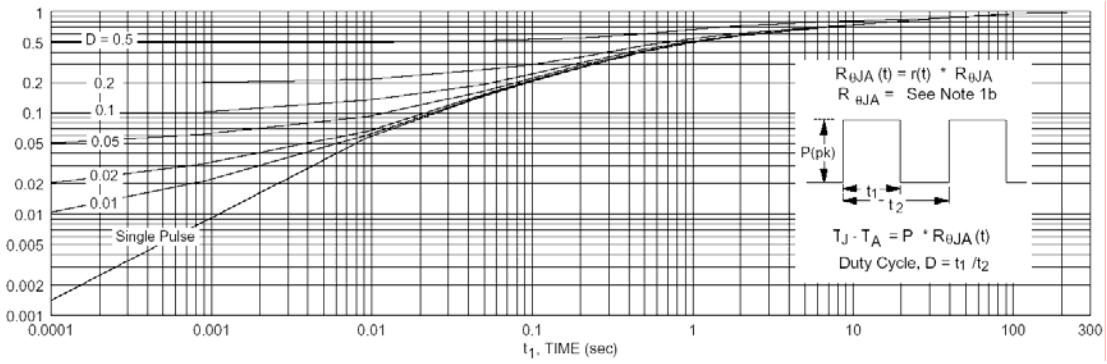
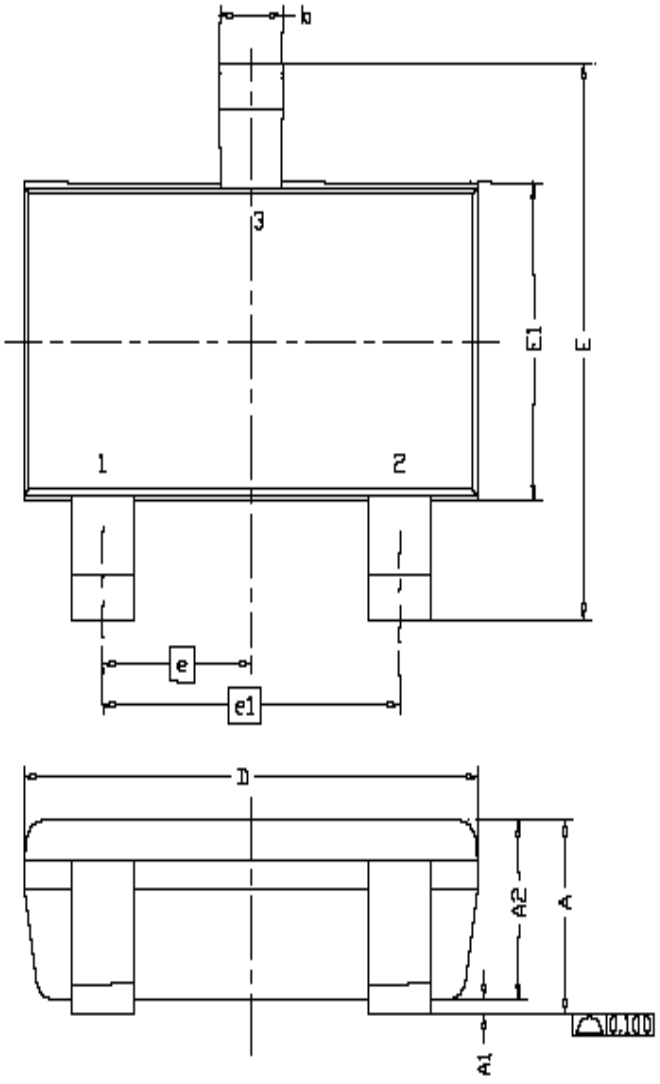


Figure 11. Transient Thermal Response Curve.

Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM