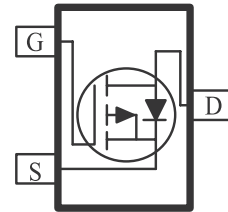
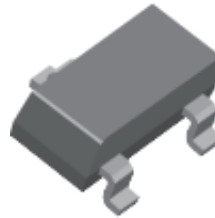


P - Channel Logic Level MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are voltage control small signal switch, power management in portable and battery-powered products and most low current high side switch.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Fast Switch
- Low Gate Charge
- High Saturation Current
- Miniature SOT-23 Surface Mount Package Saves Board Space



PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-60	10 @ $V_{GS} = -10$ V	-0.2
	20 @ $V_{GS} = -4.5$ V	-0.12

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	± 0.12	A
	$T_A = 70^\circ\text{C}$		± 0.09	
Pulsed Drain Current ^b		I_{DM}	± 1	
Continuous Source Current (Diode Conduction) ^a		I_S	0.24	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	0.36	W
	$T_A = 70^\circ\text{C}$		0.29	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{THJA}	350	$^\circ\text{C/W}$
	Steady-State		400	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Switch Off Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -10 μA	-60			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -48 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -48 V, V _{GS} = 0 V, T _J = 55°C			-150	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±10	nA
Switch On Characteristics						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 mA	-1.0	-1.7	-3.5	V
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-0.6			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -10 V, I _D = -0.5 A		1	10	Ω
		V _{GS} = -10 V, I _D = -0.5 A T _J = 55°C		1.5	12	
		V _{GS} = -4.5 V, I _D = -0.25 A		1.3	20	
Forward Tranconductance ^A	g _{fs}	V _{DS} = -5 V, I _D = -1.1 A	75	435		mS
Diode Forward Voltage	V _{SD}	I _S = 0.4 A, V _{GS} = 0 V		-0.80	-1.5	V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = -48 V, V _{GS} = -10 V, I _D = -0.5 A		1.8	2.5	nC
Gate-Source Charge	Q _{gs}			0.3		
Gate-Drain Charge	Q _{gd}			0.4		
Switching						
Turn-On Delay Time	t _{d(on)}	V _{DS} = -25 V, I _D = -0.5 A, R _G = 6 Ω, V _{GEN} = -10 V		2.7	5.5	ns
Rise Time	t _r			6.8	13	
Turn-Off Delay Time	t _{d(off)}			10	16	
Fall-Time	t _f			7.8	16	

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics

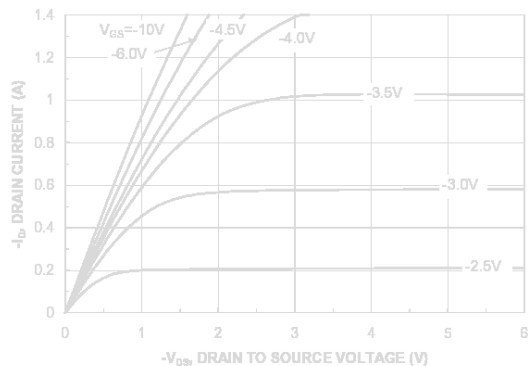


Figure 1. On-Region Characteristics

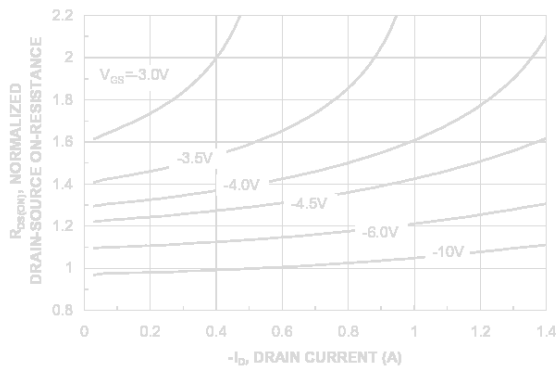


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

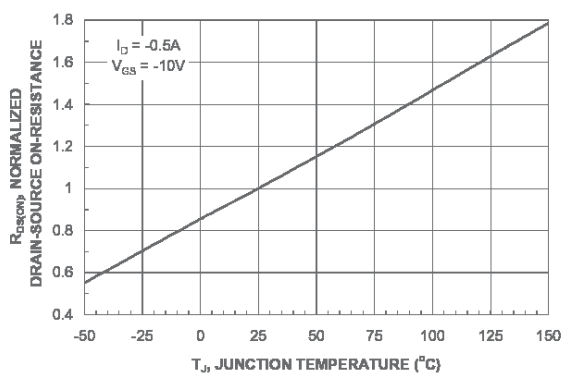


Figure 3. On-Resistance Variation with Temperature

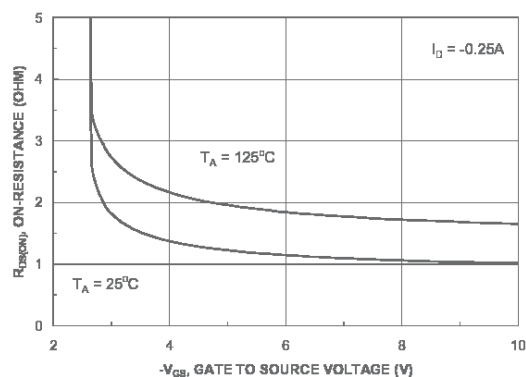


Figure 4. On-Resistance Variation with Gate to Source Voltage

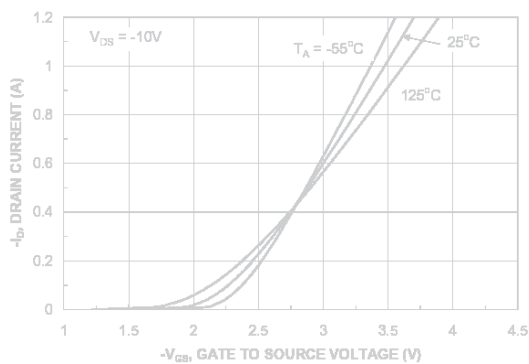


Figure 5. Transfer Characteristics

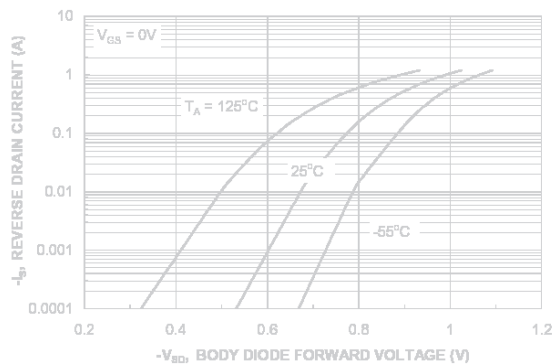


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Electrical Characteristics

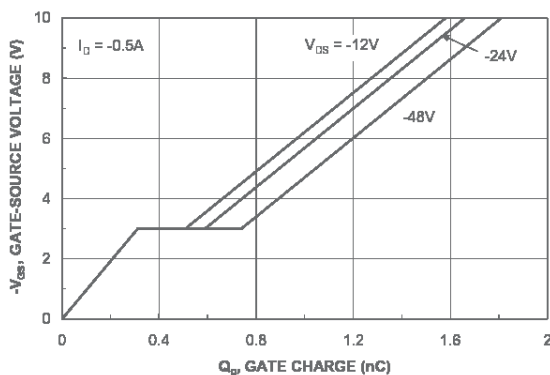


Figure 7. Gate Charge Characteristics.

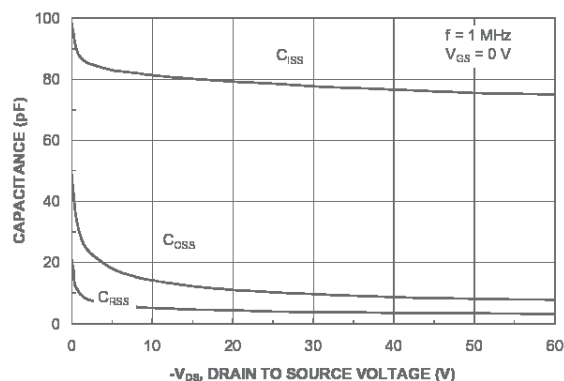


Figure 8. Capacitance Characteristics.

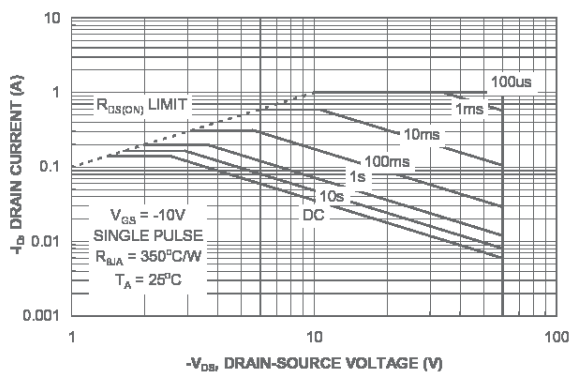


Figure 9. Capacitance Characteristic

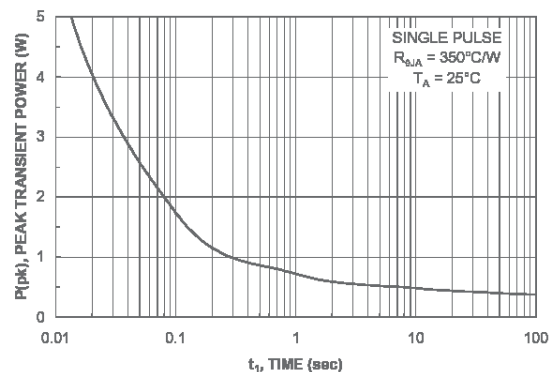


Figure 10. Gate Charge Characteristic

Normalized Thermal Transient Impedance, Junction to Ambient

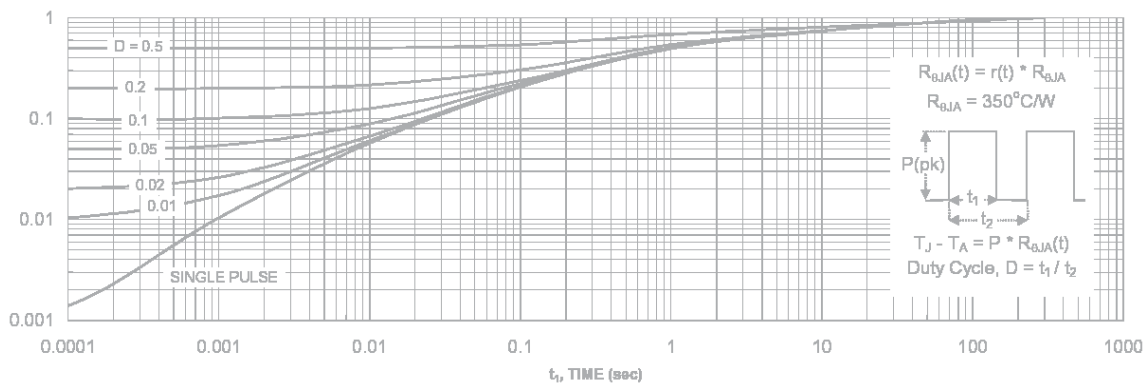
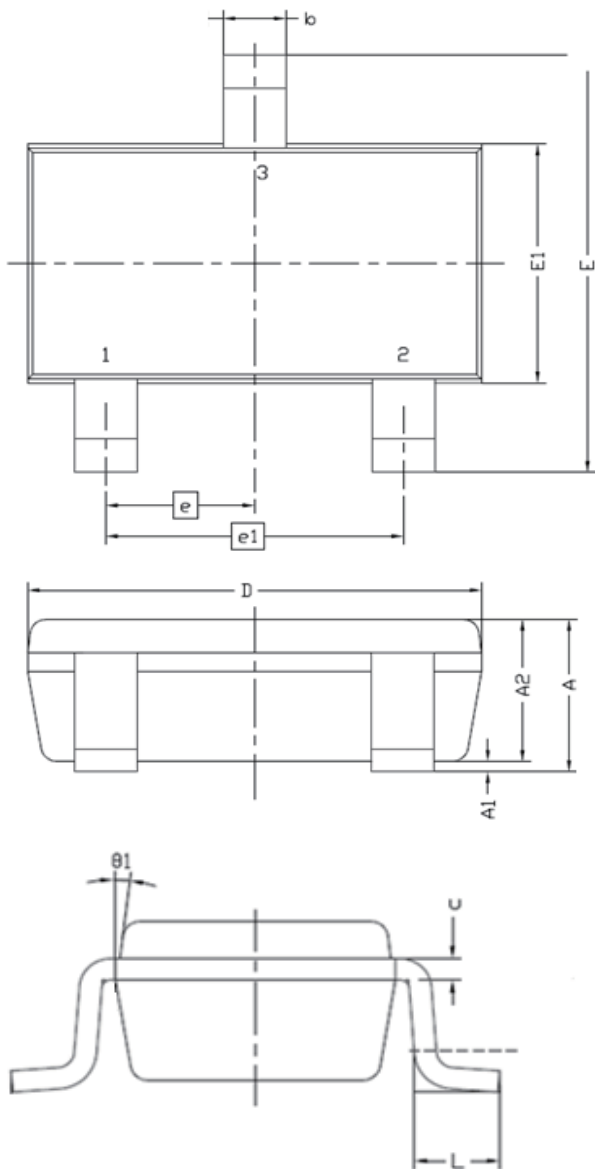


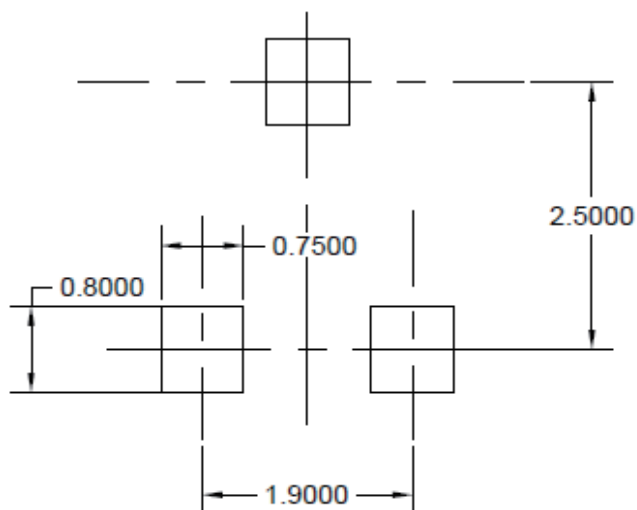
Figure 11. Transient Thermal Response Curve

Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

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