

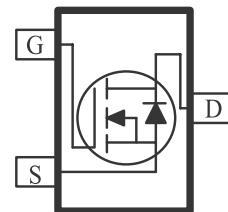
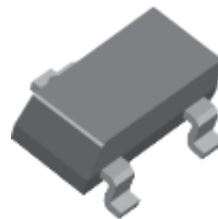
N-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT-23 Surface Mount Package Saves Board Space
- High power and current handling capability
- Low side high current DC-DC Converter applications

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
30	58 @ $V_{GS} = 10V$	3.5
	82 @ $V_{GS} = 4.5V$	3.0



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ\text{C}$	I_D	3.5	A
	$T_A = 70^\circ\text{C}$		2.8	
Pulsed Drain Current ^b		I_{DM}	16	
Continuous Source Current (Diode Conduction) ^a		I_S	1.25	A
Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	1.3	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	100	$^\circ\text{C/W}$
	Steady-State		166	$^\circ\text{C/W}$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	uA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	6			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 3.5 A			58	mΩ
		V _{GS} = 4.5 V, I _D = 3 A			82	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 3.5 A		6.9		S
Diode Forward Voltage	V _{SD}	I _S = 2.3 A, V _{GS} = 0 V		0.8		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 3.5 A		2.2		nC
Gate-Source Charge	Q _{gs}			0.5		
Gate-Drain Charge	Q _{gd}			0.8		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω , I _D = 1 A, V _{GEN} = 10 V		16		nS
Rise Time	t _r			5		
Turn-Off Delay Time	t _{d(off)}			23		
Fall-Time	t _f			3		

Notes

- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Typical Electrical Characteristics (N-Channel)

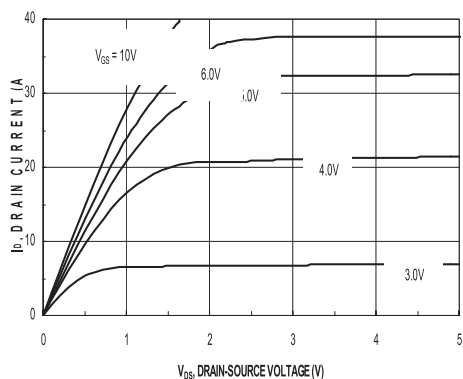


Figure 1. On-Region Characteristics

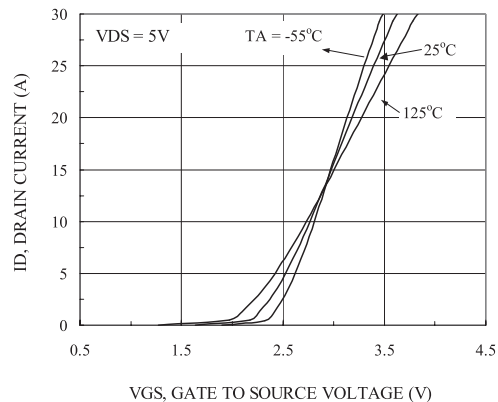


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

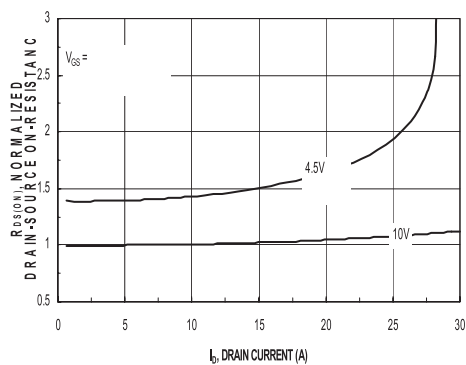


Figure 3. On Resistance Vs V_{GS} Voltage

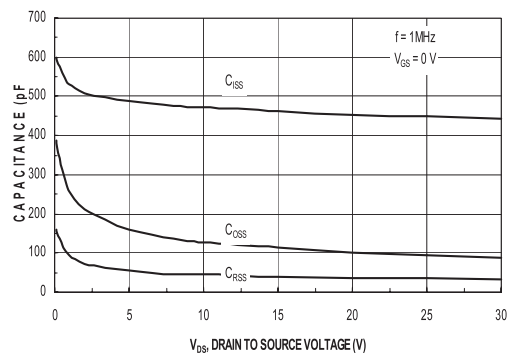


Figure 4. Capacitance Characteristics

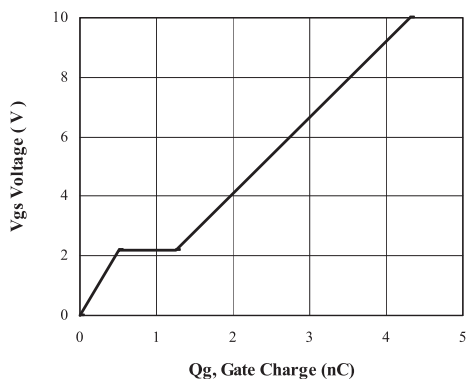


Figure 5. Gate Charge Characteristics

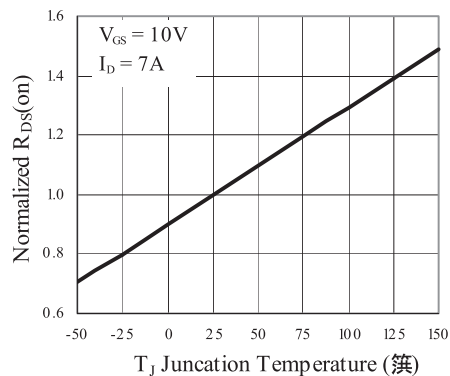


Figure 6. On-Resistance Variation with Temperature

Typical Electrical Characteristics (N-Channel)

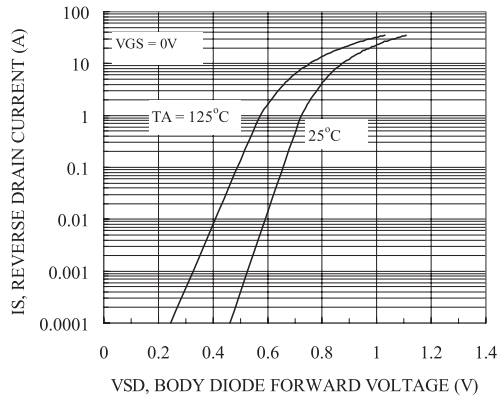


Figure 7. Transfer Characteristics

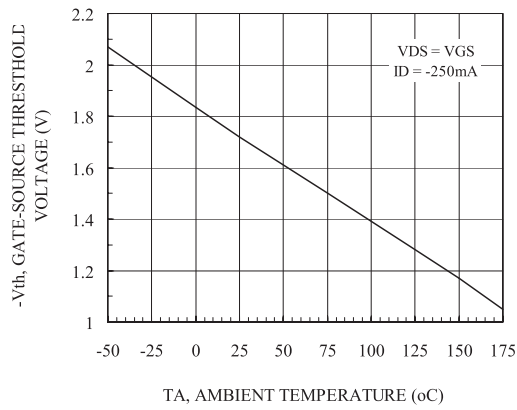


Figure 9. Vth Gate to Source Voltage Vs Temperature

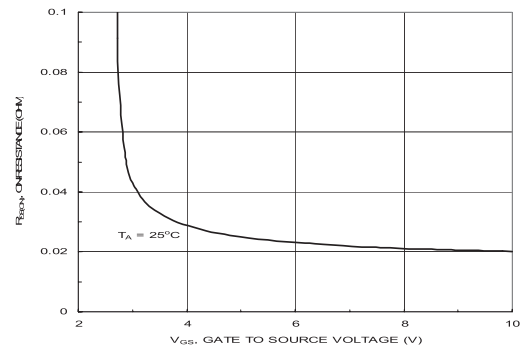


Figure 8. On-Resistance with Gate to Source Voltage

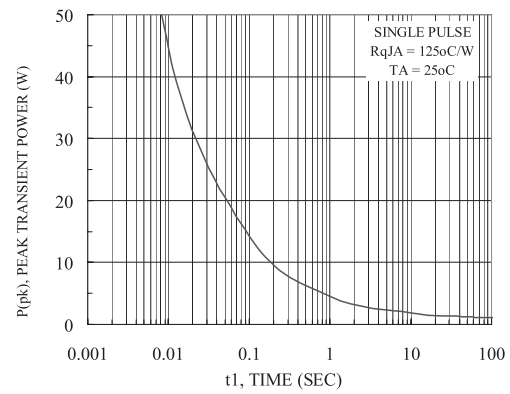


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

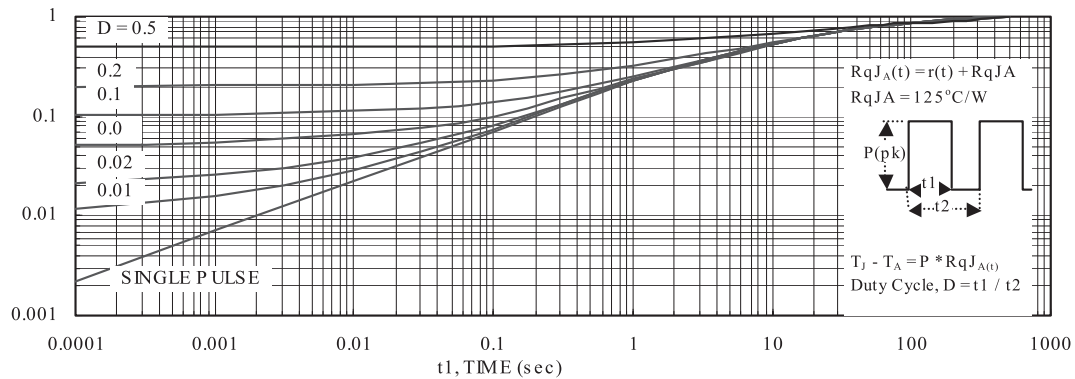
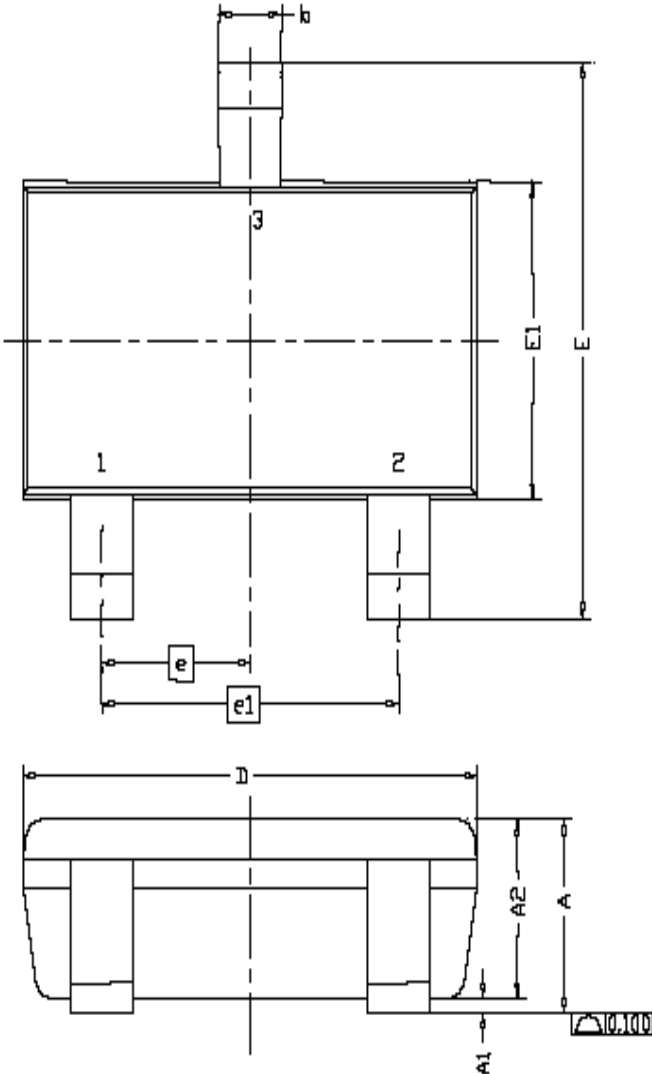
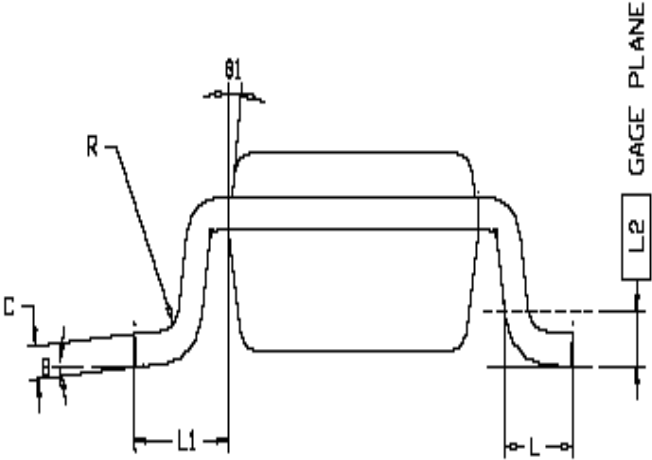


Figure 11. Transient Thermal Response Curve

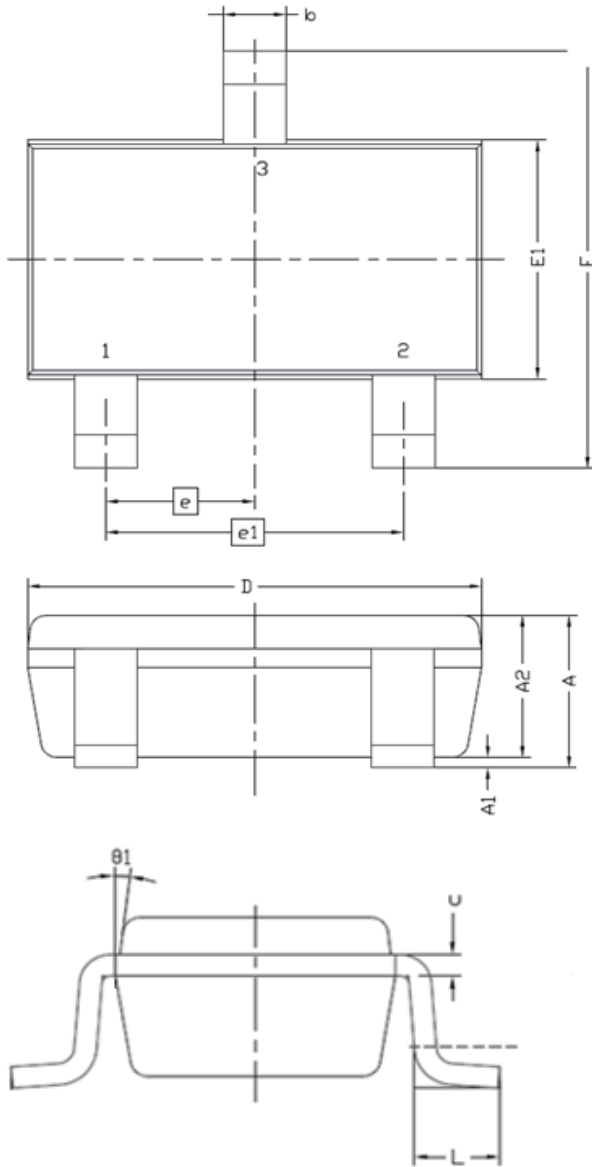
Package Information



DIM.	MILLIMETERS		
	MIN	NOM	MAX
A	0.935	0.95	1.10
A1	0.01	---	0.10
A2	0.85	0.90	0.925
b	0.30	0.40	0.50
c	0.10	0.15	0.25
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L1	0.60REF		
L2	0.25BSC		
R	0.10	---	---
θ	0°	4°	8°
θ1	7°NOM		

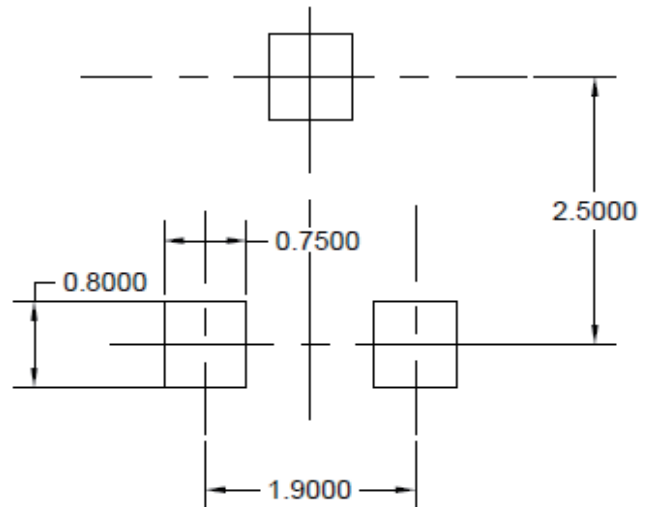


Package Information



Symbol	MILLIMETERS	
	MIN	MAX
A	0.8	1.2
A1	0	0.1
A2	0.7	1.1
b	0.3	0.5
c	0.1	0.2
D	2.7	3.1
E	2.6	3
E1	1.4	1.8
e	0.95 BSC	
e1	1.9 BSC	
L	0.3	0.6
θ1	7° NOM	

Recommended Pad Layout



Note: Drain opening is recommended to be solder mask defined in a copper fill for improved thermal performance

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.