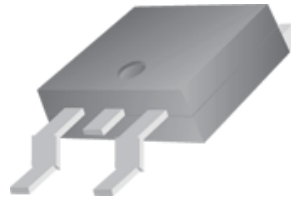


N-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
60	94 @ $V_{GS} = 10V$	19
	109 @ $V_{GS} = 4.5V$	18

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_C=25^\circ\text{C}$ I_D	19	A
Pulsed Drain Current ^b	I_{DM}	40	
Continuous Source Current (Diode Conduction) ^a	I_S	30	A
Power Dissipation ^a	$T_C=25^\circ\text{C}$ P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$

Notes

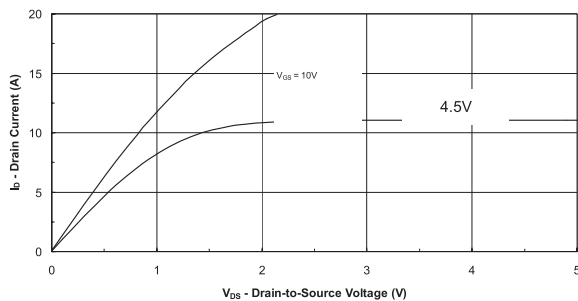
- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 uA	1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48 V, V _{GS} = 0 V			1	uA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	34			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 10 V, I _D = 19 A			94	mΩ
		V _{GS} = 4.5 V, I _D = 18 A			109	
Forward Tranconductance ^A	g _{fs}	V _{DS} = 15 V, I _D = 19 A		22		S
Diode Forward Voltage	V _{SD}	I _S = 24 A, V _{GS} = 0 V		1.1		V
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 19 A		3.6		nC
Gate-Source Charge	Q _{gs}			1.8		
Gate-Drain Charge	Q _{gd}			1.3		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 25 V, R _L = 25 Ω , I _D = 24 A, V _{GEN} = 10 V		16		nS
Rise Time	t _r			5		
Turn-Off Delay Time	t _{d(off)}			23		
Fall-Time	t _f			3		
Source-Ddrain Reverse Recovery Time	t _{rr}	I _F = 24 A, Di/Dt = 100 A/uS		50		

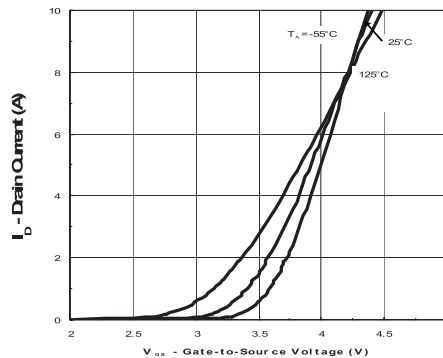
Notes

- Pulse test: $PW \leq 300 \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

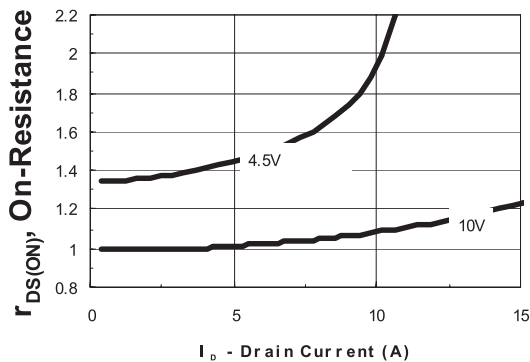
Typical Electrical Characteristics



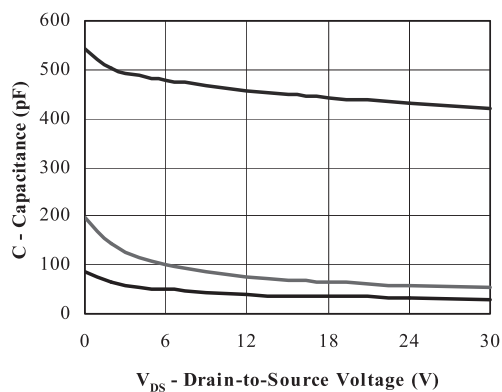
Output Characteristics



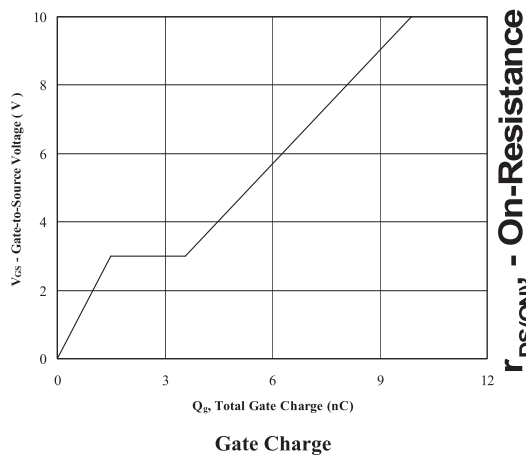
Transfer Characteristics



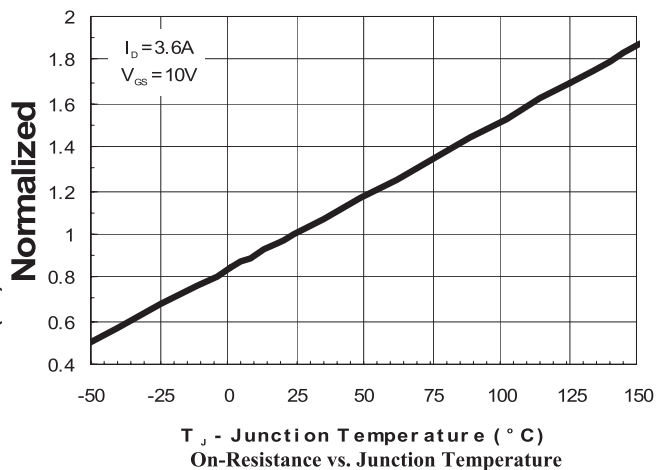
On-Resistance vs. Drain Current



Capacitance

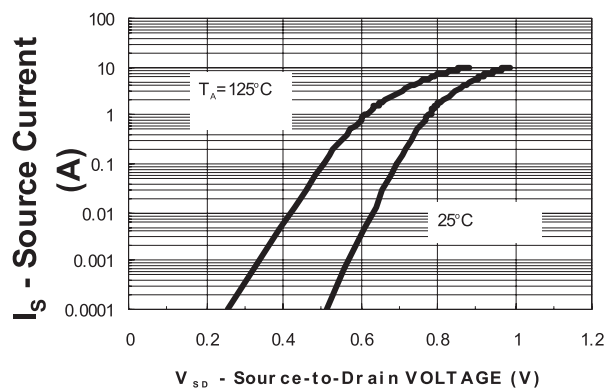


Gate Charge

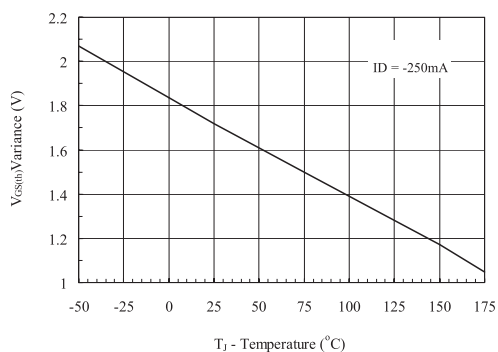


On-Resistance vs. Junction Temperature

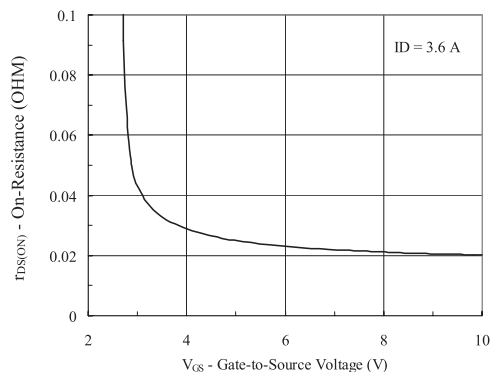
Typical Electrical Characteristics



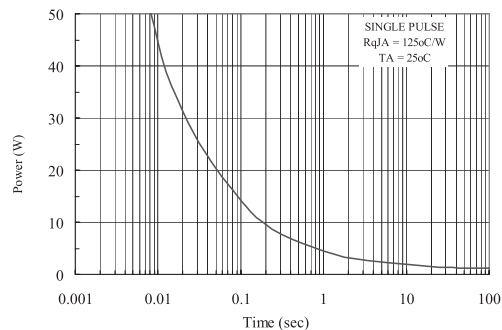
Source-Drain Diode Forward Voltage



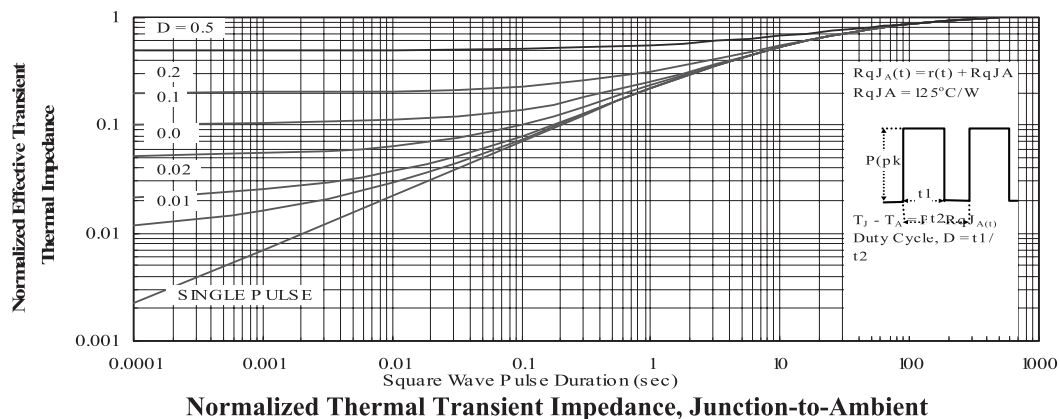
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

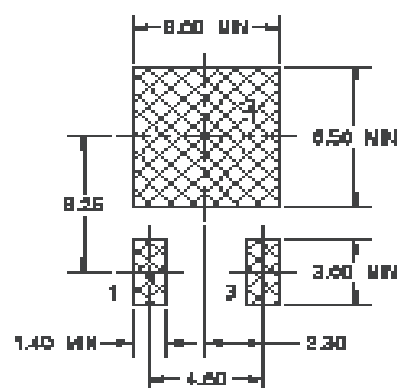
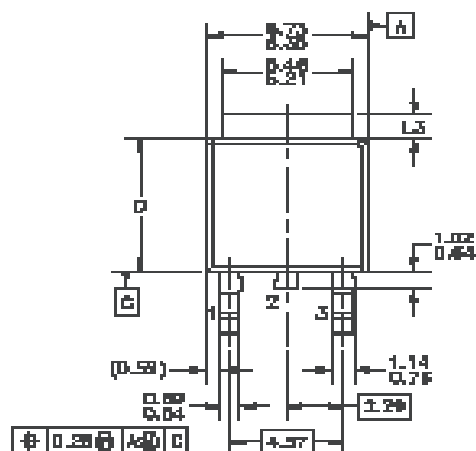


Single Pulse Power

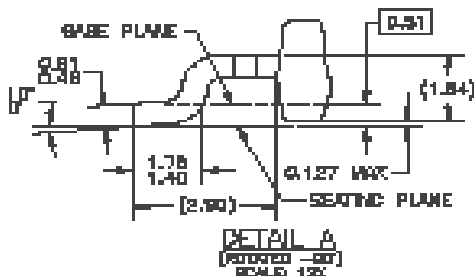
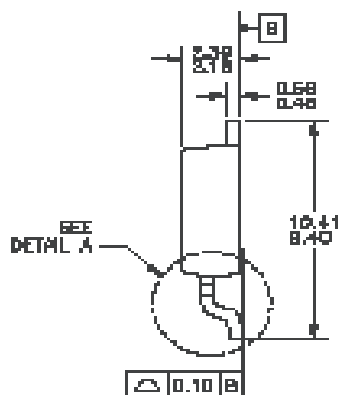
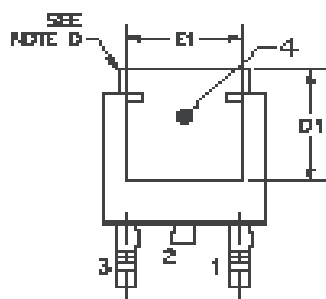


Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- ALL DIMENSIONS ARE IN MILLIMETERS.
 - THIS PACKAGE CONFORMS TO JEDEC, TO-263, ISSUE C, VARIATION AA, 30 DEC, DATED NOV. 1989.
 - DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
 - HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - DIMENSIONS L3, D, E1 & D1 TABLE:

	OPTIONAL A1	OPTIONAL A2
L3	0.68-1.27	1.02-2.54
D	0.97-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.81 MIN	4.37 MIN