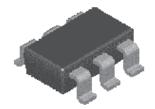
N-Channel 60V (D-S) MOSFET

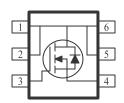
These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are power switch, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

•	Low r _{DS(on)} Provides Higher Efficiency and
	Extends Battery Life

- Low Gate Charge
- Fast Switch
- Miniature TSOP-6 Surface Mount Package Saves Board Space

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)	
60	$0.092 @ V_{GS} = 10 V$	3.4	
00	$0.107 @ V_{GS} = 4.5V$	3.1	





ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter			Maximum	Units	
Drain-Source Voltage			60	$_{ m V}$	
Gate-Source Voltage			±20	v	
Continuous Drain Current ^a	$T_A=25^{\circ}C$	1.	3.4		
Continuous Drain Current	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	ъ	2.7	Α	
Pulsed Drain Current ^b		I_{DM}	±15		
Continuous Source Current (Diode Conduction) ^a			1.7	A	
D a	$T_A=25^{\circ}C$	D_	2.0	$ $ $_{ m w}$ $ $	
Power Dissipation ^a	$T_{A}=25^{\circ}C$ $T_{A}=70^{\circ}C$	Ir D	1.3	l ^{vv}	
Operating Junction and Storage Temperature Range			-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
M	t <= 5 sec	D	62.5	00/11	
Maximum Junction-to-Ambient ^a	Steady-State	R_{THJA}	110	L/W	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Davamatav	Ch -1	T. 4 C. 122	Limits			TI24	
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \text{ uA}$	1.0			V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zara Cata Valtaga Drain Current	ī	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	,, A	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			50	uA	
On-State Drain Current ^A	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α	
Drain-Source On-Resistance ^A	r	$V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$			92	mΩ	
Drain-Source On-Resistance	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$			107		
Forward Tranconductance ^A	$g_{ m fs}$	$V_{DS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$		8		S	
Diode Forward Voltage	V_{SD}	$I_S = 1.7 \text{ A}, V_{GS} = 0 \text{ V}$		1.10		V	
Dynamic ^b							
Total Gate Charge	Q_{g}			3.6			
Gate-Source Charge	Q_{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 3.4 \text{ A}$		1.8		пC	
Gate-Drain Charge	Q_{gd}			1.3			
Turn-On Delay Time	t _{d(on)}			10			
Rise Time	$t_{\rm r}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega, I_D = 1 \text{ A},$		10			
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 \text{ V}$		20		ns	
Fall-Time	t_{f}			10			

Notes

- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.