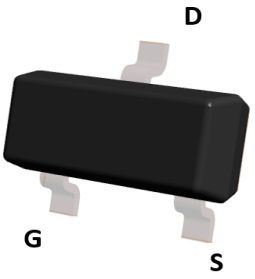
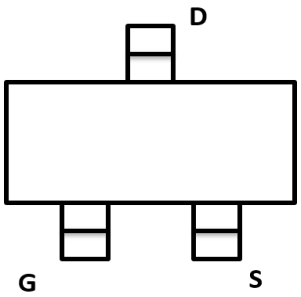
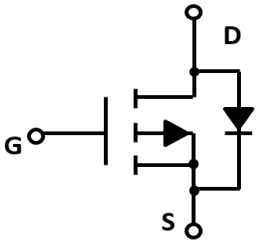
P-Channel Enhancement Mode Field Effect Transistor



Top View



SOT-23-3L



Product Summary

- V_{DS} -20V
- I_D -5.0A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜30 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜40 mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜56 mohm

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-20	V
Gate-source Voltage	V_{GS}	±10	V
Drain Current	I_D	-5.0	A
Pulsed Drain Current [A]	I_{DM}	-20	A
Total Power Dissipation @ T_A=25℃ Steady State	P_D	1.2	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]	$R_{\theta JA}$	104	℃/ W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
HAS20P7L	F2		3000	15000	180000	7” reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-18V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.7	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-5A		25	30	mΩ
		V_{GS}= -2.5V, I_D=-3A		32	40	
		V_{GS}= -1.8V, I_D=-1A		45	56	
Diode Forward Voltage	V_{SD}	I_S=-5.7A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-5	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-4V,V_{GS}=0V,f=1MHZ		740		pF
Output Capacitance	C_{oss}			290		
Reverse Transfer Capacitance	C_{rss}			190		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-2.5V,V_{DS}=-4V,I_D=-4A		4.5		nC
Gate Source Charge	Q_{gs}			1.2		
Gate Drain Charge	Q_{gd}			1.6		
Turn-on Delay Time	$t_{D(on)}$	V_{GEN}=-8V,V_{DD}=-4V, R_L=1.2Ω, I_D=-3.3A		5		ns
Turn-on Rise Time	t_r			11		
Turn-off Delay Time	$t_{D(off)}$			22		
Turn-off Fall Time	t_f			16		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

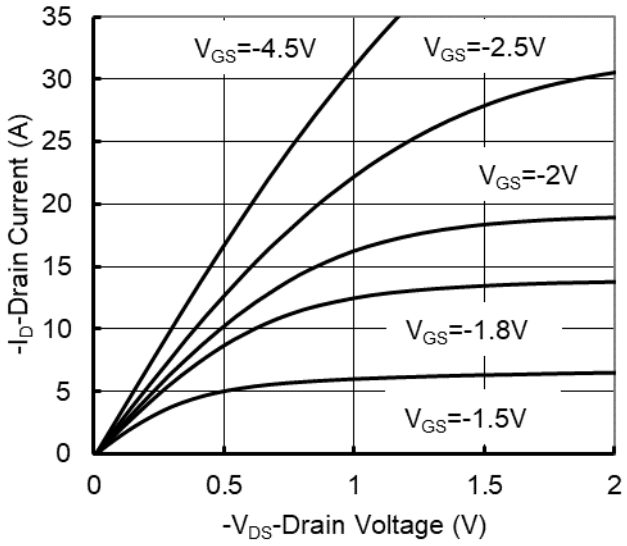


Figure1. Output Characteristics

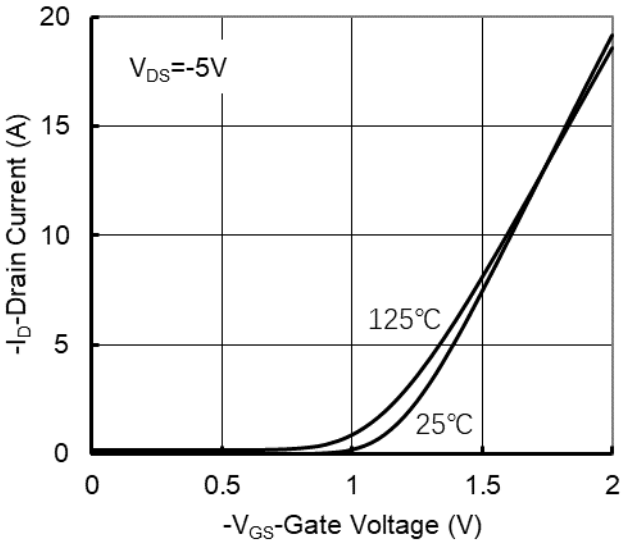


Figure2. Transfer Characteristics

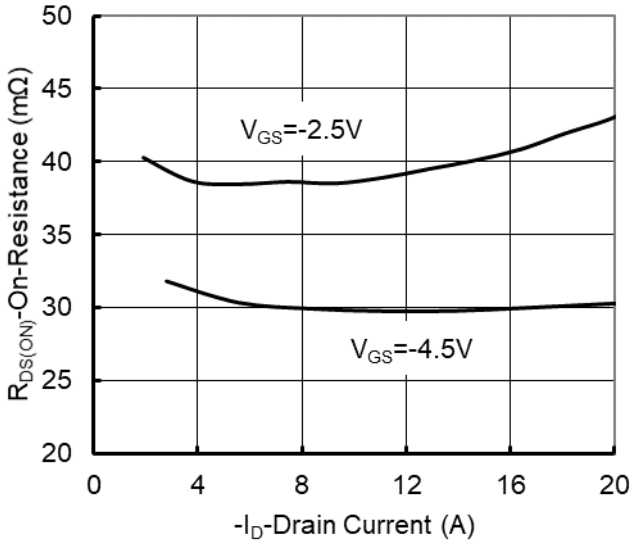


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

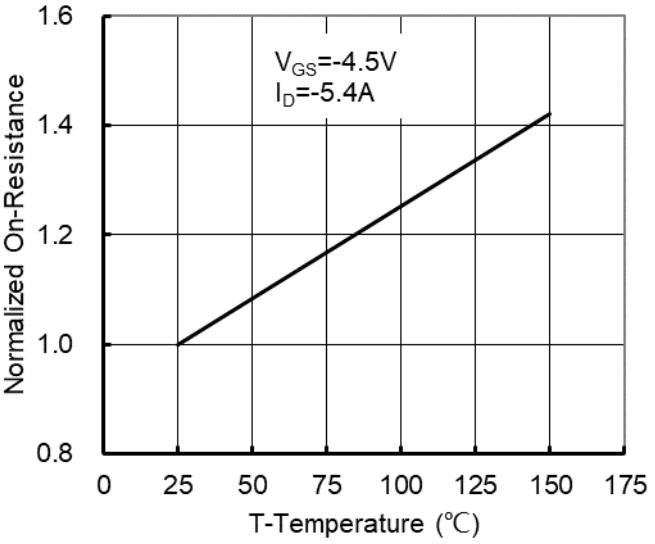


Figure 4: On-Resistance vs. Junction Temperature

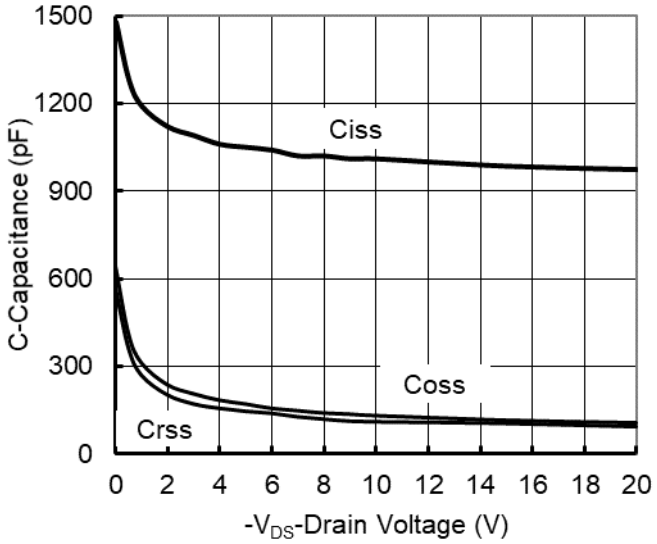


Figure5. Capacitance Characteristics

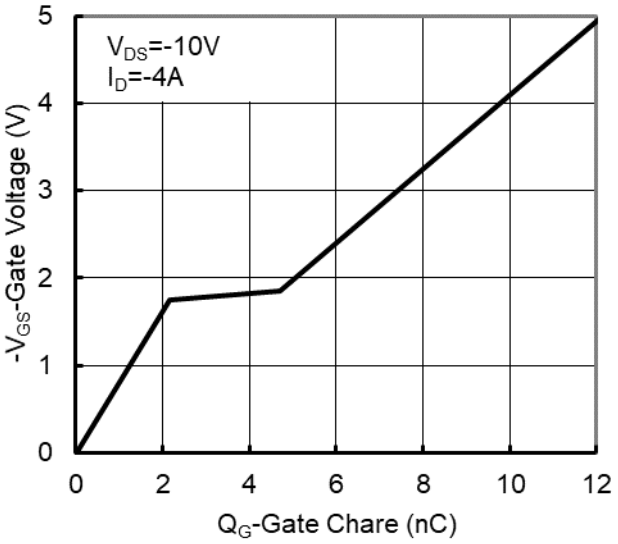


Figure6. Gate Charge

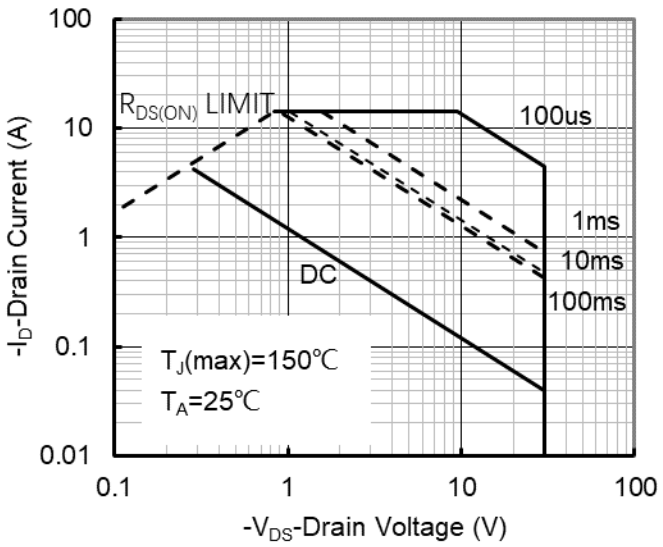


Figure7. Safe Operation Area

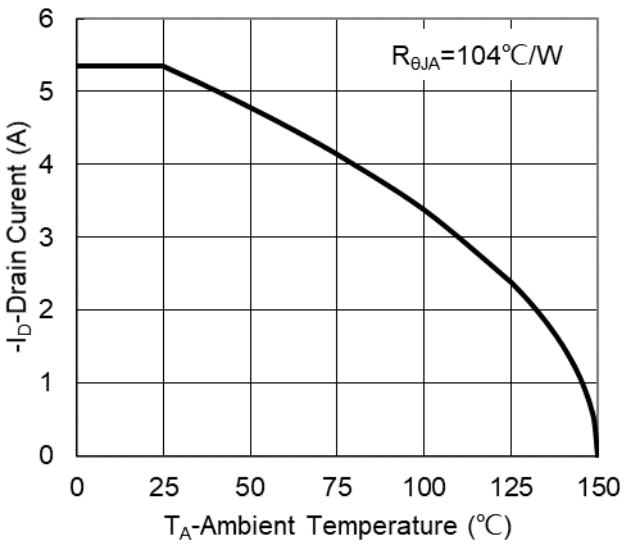
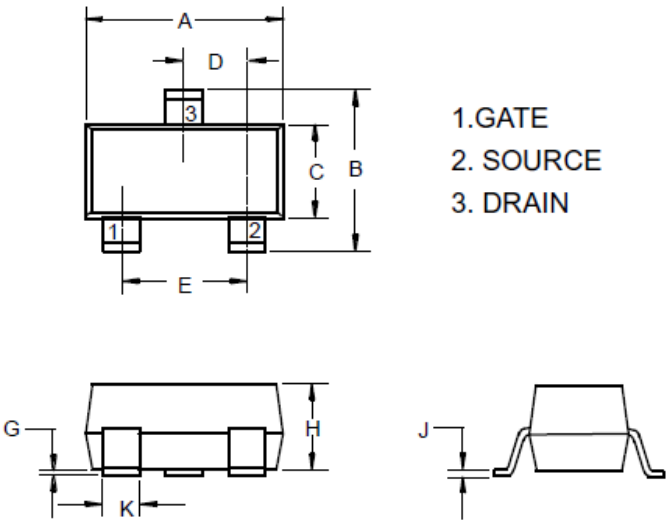


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

■ SOT-23-3L Package information

SOT-23-3L



1.GATE
2. SOURCE
3. DRAIN

DIMENSIONS					
	INCHES		MM		
DIM	MIN	MAX	MIN	MAX	NOTE
A	.113	.117	2.87	2.97	
B	.108	.112	2.75	2.85	
C	.061	.065	1.55	1.65	
D	.036	.038	.914	.965	
E	.073	.077	1.85	1.95	
G	.0016	.0039	.04	.100	
H	.044	.049	1.12	1.25	
J	.006	.007	.14	.17	
K	.013	.015	.34	.37	

■ SOT-23-3L Suggested Pad Layout